BR32F450SS

DataSheet

Rev2.1.6

CMOS
Microcontroller Unit

Revision History

Release Number	Date	Author	Summary of Changes
2.0.0	2020/07/08	BRMICRO	This version is for initial version
2.1.0	2020/08//11	BRMICRO	Adding timing
2.1.1	2020/09/04	BRMICRO	Adjust the format
2.1.2	2020/10/23	BRMICRO	Adding Package information
2.1.3	2020/11/16	BRMICRO	Adding GINT PIN
2.1.4	2021/02/18	BRMICRO	Adjust IIC3 Alternate
2.1.5	2021/02/20	BRMICRO	For BR32F450SS
2.1.6	2021/02/22	BRMICRO	Adjust the format

Section 1 Introduction

Section 2 System Memory Map

Section 3 Signal Description

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Section 1 Introduction

1.1 Introduction

- BR32F4x Series Chips are multi-purpose MCU based on the Cortex-M4F central processor unit (CPU).Internal high speed 500MHz oscillator(trim to 400MHz in typical case).
- Have a 8Mbyte SDRAM stacked on the chip
- The temperature range is of -25^{O}C to 85^{O}C.The operating frequency is up to 500MHz at typical condition.
- Chip package is:

  LQFP128

1.2 Features

- Cache
  - On-chip, 32K Bytes ICache,32K Bytes DCache.
  - Has two AHB bus interfaces, a master and a slave interface.
  - Has a 2-way set-associative organization.
  - Has an AHB bus interface to access its programmer's model.
- OnCE debug support
- On-chip, 64K Bytes of static random-access memory can only be accessed by CPU(TCMSRAM)
- On-chip, 128K Bytes of static random-access memory (SRAM):
  - Single cycle byte, half-word (16-bit), and word (32-bit) reads and writes
- On-chip, 64K Bytes of static read only memory (ROM):
  - Single cycle byte, half-word (16-bit), and word (32-bit) read access.
- On-chip embedded flash (EFLASH)
  - Memory Origanization: 256K Bytes LP
  - Read of bytes, aligned halfwords (16 bits) and aligned words (32 bits)

  - Automated program and erase operation
  - Optional interrupt on command completion
  - Data Retention: 10 years under 85 degrees
  - 0.99~1.21V/1.5~1.98V dual power supplies
- CPM
  - Multiple system clock sources
  - Separate clock divider
  - Support for power saving mode
  - Module clock can be gated separately
- Programmable 32bit Interrupt timer(PIT) :
  - 32-bit counter with modulus "initial count" register
  - Selectable as free running or count down
- Watchdog timer(WDT) :
  - 16-bit counter with modulus "initial count" register
  - Pause option for low-power modes
- Time Counter :
  - 16-bit counter with modulus "initial count" register
  - Pause option for low-power modes
- Reset :
  - Separate reset in and reset out signals
  - Five sources of reset:
    Power-on reset
    Software reset
    Watchdog timer
    Time Counter
    Power Attack Detect Reset (Low and High Voltage Detect Reset)
  - Status flag indicates source of last reset
- DMA Controller
  - Four independently programmable DMA controller channels
  - Data transfers in 8, 16, 32 ,64bits

  - Support single transfer, Burst 4, 8,16 transfer, and burst always under a speical case.
  - Support single cycle transfer
  - Support automatic transfer mode
  - Support LLI transfer mode
  - Follow a fixed priority rule
- EDMAC
  - Programmable transfer total number
  - Programmable read buffer address and write buffer address
  - Support read, write and write then read transfer
- CRC coprocessor
  - Support CRC32 / CRC16 / CRC8
  - Support DMAC Data from CRC
  - Support EDMAC Data from CRC
- External interrupts supported(EPORT) :
  - Rising/falling edge select
  - Low-level sensitive
  - Ability for software generation of external interrupt event
  - Interrupt pins configurable as general-purpose I/O
- I2C Controller
  - Supports 10 bit addressing.
  - Supports Standard Mode, Fast Mode and High-Speed Mode
  - Software option to select between High-Speed mode and Standard/Fast mode
  - Compatibility with standard and fast-mode of I2C bus version 2.1 standard.
  - Multiple-master operation.
  - Software-programmable for one of 64 different serial clock frequencies.
  - Software-selectable acknowledge bit.
  - Interrupt-driven, byte-by-byte data transfer.
  - Arbitration-lost interrupt with automatic mode switching from master to slave.

  - Transfer completion and read configure interrupt.
  - Start and stop signal generation/detection.
  - Repeated START signal generation.
  - Acknowledge bit generation/detection.
  - Bus-busy detection.
  - Option slave address receiving enable when system clock stop mode
  - SCL or SDA line gpio function supported
- Serial communications interface (SCI):
  - Full-duplex operation
  - 13-bit baud rate prescaler
  - Programmable 8-bit or 9-bit data format
  - Separately enabled transmitter and receiver
  - Separate receiver and transmitter CPU interrupt requests
  - Two receiver wakeup methods (idle line and address mark)
  - Receiver framing error detection
  - Hardware parity checking
  - 1/16 bit-time noise detection
  - General-purpose I/O capability
- Serial communications interface (SCI_TS):
  - Separate 16x9 transmit (TX) and receive (RX) FIFOs to reduce CPU interrupt service loading
  - FIFO trigger levels of 1/8, 1/4, 1/2, 3/4, and 7/8
  - Automatic hardware flow control supported
  - Serial IR interface low-speed,IrDA-compatible(up to 115.2Kbit/s)
  - Full-duplex operation
  - 13-bit baud rate prescaler
  - Programmable 8-bit or 9-bit data format
  - Separately enabled transmitter and receiver
  - Separate receiver and transmitter CPU interrupt requests
  - Two receiver wakeup methods (idle line and address mark)
  - Receiver framing error detection

  - Hardware parity checking
  - 1/16 bit-time noise detection
  - General-purpose I/O capability
- Serial peripheral interfaces (SPI) :
  - Master mode and slave mode configurable
  - Slave select output
  - Mode fault error flag with CPU interrupt capability
  - Separate transmit and receive FIFOs
  - Serial clock with programmable polarity and phase
  - Control of SPI operation during doze mode
- USBOTG1.1
  - Supports internal reference clock or external 12MHz crystal reference clock
  - Performs all transaction scheduling in hardware
  - Operates either as a function controller for a USB peripheral or as the host/peripheral in point-to-point communications with another USB function
  - Synchronous RAM interface for FIFOs
  - Supports point-to-point communications with one full-speed device
  - Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
  - Supports Suspend and Resume
  - Configurable for up to 15 additional Transmit endpoints and up to 15 additional Receive endpoints
  - Configurable FIFOs, including the option of dynamic FIFO sizing
  - Support for DMA access to FIFOs
- Soft connect/disconnect option PWM
  - Programmable period
  - Programmable duty cycle
  - Two Dead-Zone generator
  - Capture function
  - Pins can be configured as general-purpose I/O

- PWMT
  - 16-bit up, down, up/down auto-reload counter
  - 16-bit programmable prescaler allowing dividing (also “on the fly”) the counter clock frequency either by any factor between 1 and 65536
  - Up to 4 independent channels
  - Complementary outputs with programmable dead-time
  - Synchronization circuit to control the timer with external signals and to interconnect several timers together
  - Repetition counter to update the timer registers only after a given number of cycles of the counter
  - Interrupt/DMA generation on the some events
- Controller Area Network (CAN):
  - Full implementation of the CAN protocol specification, version 2.0B
  - Flexible Message Buffers (up to 64) of zero to eight bytes data length
  - Programmable loop-back mode supporting self-test operation
  - Time Stamp based on 16-bit free-running timer
  - Global network time, synchronized by a specific message
  - Maskable interrupts
- Ethernet MAC:
  - Compliant with RMII
  - Include internal DMA
  - Include RXFIFO and TXFIFO
  - Maskable interrupts
  - Automatic receiving data according to the actual length of the frame
- SD_HOST 2.0:
  - Supports Secure Digital I/O protocol commands
  - Supports Command Completion signal and interrupt to host processor
  - Single-channel; single engine used for Transmit and Receive, which are mutually exclusive
  - Fully synchronous design operating on a single system clock
  - Dual-buffer and chained descriptor linked list
  - Programmable interrupt options for different operational conditions

- ADC
  - 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
  - ADC conversion time: 1.0 μs for 12-bit resolution (1 MHz), 0.88 μs conversion time for 10 bit resolution, faster conversion times can be obtained by lowering resolution.
  - Programmable sampling time
  - DMA support
- DAC
  - Left or right data alignment
  - DMA capability
  - External triggers for conversion
  - Programmable internal buffer
  - Input voltage reference, VDDA
  - FIFO Based operation
- Secure features
  - Internal power on reset
  - Voltage detector
  - Ligth detector
  - Power Glitch detector
  - Metal Shield protection
  - Temperature detector
  - Data encryption
  - Clock and reset pulse filtration
  - Safe optimized routing
- Crypto Accelerator module
  - Large operand size N integer arithmetic

    32 * R bits

    R is positive integer from 1 to 64
  - Programmable scalar or modulo operation

    Y = (A * B) mod M

    Y = (A^E) mod M

  - Discrete "sea-of-gates" implementation to protection against SPA and probing attacks
- AES module
  - Support AES encryption/decryption algorithm
  - Support AES algorithm with 128/192/256 bits key
  - Support Electronic Code Book (ECB) mode operation and CTR(counter) mode operation
- SHA coprocessor
  - SM3(256)
  - SHA-0(160)
  - SHA-1(160)
  - SHA-224(224)
  - SHA-256(256)
  - SHA-384(384)
  - SHA-512(512)
  - Share hardware between different SHA processing
- SM4 module
  - Support sm4 encryption/decryption algorithm.
  - Support sm4 algorithm with 128 bits key
  - Support ECB and CBC mode
  - Support MLBBUS Interface
- DES coprocessor
  - Support DES and Triple-DES encryption and decryption algorithm
  - Support DES algorithm with 64(56) bits key
  - Support Triple-DES algorithm with 128(112) bits or 192(168) bits key
  - Support ECB mode and CBC mode
  - Support MLBBUS Interface
- TRNG(random number generator)
  - Max Rate: 20Mbps
- PMU_RTC
  - Internal 32KHz oscillator

  - Load time data to and read time data from seconds, minutes, hours and days counters
  - Support alarm settings
  - Interrupt sources:second, minute, hour,day interrupts,programmable alarm interrupts ,1KHZ/32KHZ periodic interrupts .
- PXLP
  - Single AHB master bus architecture
  - User programmable offset for sources and destination areas of picture for dma
  - User programmable sources and destination addresses on the whole memory space
  - Copy from an area to another
  - Support average filter algorithm
  - Support histogram algorithm
  - Support hough algorithm
  - Support Reed-Solomon(RS) error correction algorithm
  - Support binary image
  - Support look for Minmum value,Maxmum value and computing average value in the block(Min_MAX_Average, MMA),The image split number of blocks is no more than 32. Support user programmable the block size.
  - Look for Minmum value,Maxmum value and computing average value in the block(Min_MAX_Average, MMA), support the image data from Digital Camera Interface (DCMI) directly.
  - Support black white run length coding algorithm
  - Interrupt generation on process completion
  - Support YOLO v3 deep learning end-to-end real-time target detection algorithm
  - Darknet light open source deep learning framework realized by YOLO v3, with less dependence and good portability. Due to its outstanding ability of speed and precision, especially small object detection, Darknet is widely used at present
- LCDC
  - compliance to the *AMBA Specification (Rev 2.0)* onwards for easy integration into SoC implementation

  - dual 16-deep programmable 32-bit wide FIFOs for buffering incoming display
  - data
  - supports single and dual panel mono *Super Twisted Nematic* (STN) displays with 4 or 8-bit interfaces
  - supports single and dual-panel color and monochrome STN displays
  - supports *Thin Film Transistor (*TFT) color displays
  - resolution programmable up to 1024 x 768
  - 15 gray-level mono, 3375 color STN, and 32K color TFT support
  - 1, 2, or 4 *bits-per-pixel* (bpp) palettized displays for mono STN
  - 1, 2, 4 or 8 bpp palettized color displays for color STN and TFT
  - 16 *bits-per-pixel* (bpp) true-color non-palettized, for color STN and TFT
  - programmable timing for different display panels
  - 256 entry, 16-bit palette RAM, arranged as a 128 x 32-bit RAM physically
  - frame, line and pixel clock signals
  - AC bias signal for STN and data enable signal for TFT panels
  - patented gray scale algorithm
  - supports little and big-endian, as well as WinCE data formats.
  - supports gamma correction
  - supports rgb565 output
- DCMI
  - 8-bit parallel interface(DVP)
  - Embedded/external line and frame synchronization
  - Continuous or snapshot mode
  - Crop feature
  - Supports the following data formats:
  - 8- bit progressive video: either monochrome or raw bayer
  - YCbCr 4:2:2 progressive video and gray output
  - YCbCr 4:2:0 directly output and gray output
  - RGB 565 progressive video and gray output
  - Compressed data: JPEG

  - Supports internal DMA and external DMA for RGB and gray data output simultaneously
  - Supports internal DMA and external DMA exchangable
  - Supports MIPI-IPI format
  - Supports Crop for gray window
- SSI
  - Serial-master operation
  - DMA controller interface – Enables the SSI to interface to a DMA controller over the bus using handshaking interface for transfer requests.
  - Clock stretching support in enhanced SPI transfers
  - Data item size (4 to 32 bits) – Item size of each data transfer under control of the programmer
  - FIFO depth – Configurable depth of the transmit and receive FIFO buffers from 2 to 256 words deep. The FIFO width is fixed at 32 bits
  - Enhanced SPI support
  - Execute in Place (XIP) mode support
- GPIO
  - Support 81 GPIO

1.3 Block Diagram

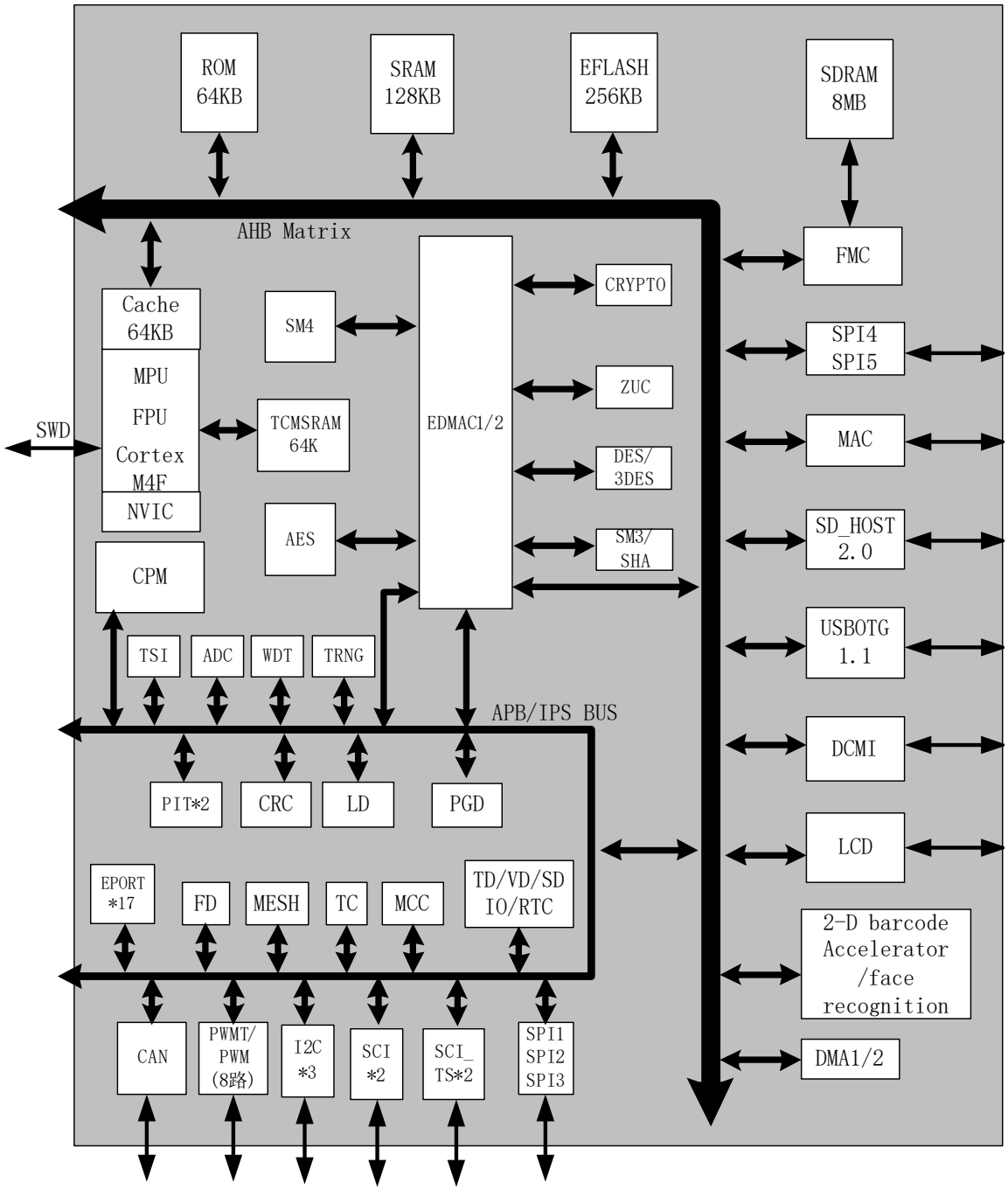

Figure 1-1 Block Diagram

Section 2 System Memory Map

2.1 Introduction

The address map, shown in **2.2**, includes:

- 64K Bytes of internal read only memory (ROM)
- 128K Bytes of internal static random-access memory (SRAM)
- 64K Bytes TCMSRAM
- 256K Bytes EFLASH
- 8M Bytes SDRAM
- Internal memory mapped registers

2.2 Address Map

Table 2-1 Boot Modes

mode[1]	mode[0]	Boot mode	Aliasing
0	0	ROM	ROM is selected as the boot space
0	1	EFLASH	EFLASH is selected as the boot space
1	0	SDRAM	SDRAM is selected as the boot space
1	1	SPI FLASH	SPI FLASH is selected as the boot space

Table 2-2 Memory mapping vs Boot mode/physical remap

Address	Boot/Remap in ROM	Boot/Remap in EFLASH	Boot/Remap in SDRAM	Boot/Remap in SPI FLASH
0xA4000000~ 0xA7FFFFFF	SDRAM2LCD	SDRAM2LCD	SDRAM2LCD	SDRAM2LCD
0x80000000~ 0x87FFFFFF	SDRAM	SDRAM	SDRAM	SDRAM
0x20000000~ 0x2001FFFF	SRAM	SRAM	SRAM	SRAM
0x1FFF0000~ 0x1FFFFFFF	TCMSRAM	TCMSRAM	TCMSRAM	TCMSRAM
0x18000000~ 0x1BFFFFFF	SDRAM (Cached)	SDRAM (Cached)	SDRAM (Cached)	SDRAM (Cached)

Table 2-2 Memory mapping vs Boot mode/physical remap

0x14000000~ 0x17FFFFFF	SPI2 FLASH (Cached)	SPI2 FLASH (Cached)	SPI2 FLASH (Cached)	SPI2 FLASH (Cached)
0x10000000~ 0x13FFFFFF	SPI1 FLASH (Cached)	SPI1 FLASH (Cached)	SPI1 FLASH (Cached)	SPI1 FLASH (Cached)
0x08000000~ 0x0803FFFF	EFLASH	EFLASH	EFLASH	EFLASH
0x04000000~ 0x0400FFFF	ROM	ROM	ROM	ROM
0x00000000~ 0x03FFFFFF	ROM(64K) Aliased	EFLASH(256K) Aliased	SDRAM(16M) Aliased	SPI4(64M) Aliased

Table 2-3 Register Address Location Map

0x4000_0000	4Kbyte	AHB_IPS1	IO Control Module(IOCTRL)
0x4000_1000	4Kbyte		Chip configuration (CCM)
0x4000_2000	4Kbyte		Reset (RESET)
0x4000_3000	4Kbyte		TFM
0x4000_4000	4Kbyte		CPM
0x4000_5000	4Kbyte		Watchdog timer (WDT)
0x4000_6000	4Kbyte		TC
0x4000_7000	4Kbyte		PIT1
0x4000_8000	4Kbyte		PIT2
0x4000_9000	4Kbyte		Edge Port 16(EPORT16)
0x4000_a000	4Kbyte		EDMAC1
0x4000_b000	4Kbyte		Edge Port 14(EPORT14)
0x4000_c000	4Kbyte		Edge Port 15(EPORT15)
0x4000_d000	4Kbyte		PIT3
0x4000_e000	4Kbyte		PIT4
0x4000_f000	4Kbyte		CAN
0x4001_0000	4Kbyte		SPI1
0x4001_1000	4Kbyte		SPI2
0x4001_2000	4Kbyte		SPI3
0x4001_3000	4Kbyte		SCI1
0x4001_4000	4Kbyte		SCI2
0x4001_5000	4Kbyte		Reserved
0x4001_6000	4Kbyte		USI3
0x4001_7000	4Kbyte		I2C
0x4001_8000	4Kbyte		PWM
0x4001_9000	4Kbyte		Edge Port (EPORT)
0x4001_a000	4Kbyte		Edge Port 1(EPORT1)
0x4001_b000	4Kbyte		I2C2
0x4001_c000	4Kbyte		I2C3
0x4001_d000	4Kbyte		SCI_TS1

0x4001_e000	4Kbyte	AHB_IPS1	SCI_TS2
0x4001_f000	4Kbyte		PWMT
0x4002_0000	4Kbyte		ADC
0x4002_1000	4Kbyte		DAC
0x4002_2000	4Kbyte		MCC
0x4002_3000	4Kbyte		TSI
0x4002_4000	4Kbyte		Edge Port 2(EPORT2)
0x4002_5000	4Kbyte		Edge Port 3(EPORT3)
0x4002_6000	4Kbyte		Edge Port 4(EPORT4)
0x4002_7000	4Kbyte		Edge Port 5(EPORT5)
0x4002_8000	4Kbyte		Edge Port 6(EPORT6)
0x4002_9000	4Kbyte		Edge Port 7(EPORT7)
0x4002_a000	4Kbyte		Edge Port 8(EPORT8)
0x4002_b000	4Kbyte		Edge Port 9(EPORT9)
0x4002_c000	4Kbyte		Edge Port 10(EPORT10)
0x4002_d000	4Kbyte		Edge Port 11(EPORT11)
0x4002_e000	4Kbyte		Edge Port 12(EPORT12)
0x4002_f000	4Kbyte		Edge Port 13(EPORT13)
0x4003_0000	4Kbyte		LD
0x4003_1000	4Kbyte		True Random Number Generator (TRNG)
0x4003_2000	4Kbyte		PGD
0x4003_3000	4Kbyte		SEC_DET
0x4003_4000	4Kbyte		PCI
0x4003_5000	4Kbyte		PMU_RTC
0x4003_6000	4Kbyte	AHB_IPS2	Reserved
0x4003_7000	4Kbyte		CRYPTO
0x4003_8000	4Kbyte		SHA
0x4003_9000	4Kbyte		EDMAC0
0x4003_a000	4Kbyte		Reserved
0x4004_0000	4Kbyte	AHB1(AHB_CLB)	Data Encryption Standard Module (DES)
0x4004_1000	4Kbyte		AES
0x4004_2000	4Kbyte		SM4
0x4004_3000	4Kbyte		ZUC
0x4004_4000	4Kbyte	AHB2	CRC0
0x4004_5000	4Kbyte		CRC1
0x4004_6000	4Kbyte		DMAC1
0x4004_7000	4Kbyte		DMAC2
0x4004_8000	4Kbyte		CLCD
0x4004_9000	4Kbyte		TRNG_OSC
0x4004_a000	4Kbyte		SD_HOST

0x4004_c000	4Kbyte	AHB3	USBC
0x4005_0000	4Kbyte	AHB_APB	MIPI
0x4005_1000	4Kbyte		Cache_Config
0x4005_2000	4Kbyte		DMA2D
0x4005_3000	4Kbyte		DCMI
0x4005_4000	4Kbyte		PXLP
0x4005_5000	4Kbyte		Cache2_Config
0x4005_6000	4Kbyte		DCMI_DVP
0x4005_7000	4Kbyte		I2S
0x4006_0000	64Kbyte	AHB_MAC	MAC
0x6000_0000	4Kbyte	AHB_SPI4	SPI4
0x7000_0000	4Kbyte	AHB_SPI5	SPI5
0x9c00_0000	4Kbyte	AHB_SDRAM	SDRAM
0xa800_0000	4Kbyte	AHB_SDRAM2LCD	SDRAM2LCD
0xe000_0000	4Kbyte	M4	M4 SYS

System Memory Map

Section 3 Signal Description

3.1 Introduction

The chip is available in package:

- LQFP128 (including 8MB SDRAM)

3.2 Package Pinout Summary

3.3 Signal Properties Summary

below is the signal description.

Table 3-1 Signal Description

Pin No.	Name[1]	Alternate	Dir.	Power	Default Pull[2,3]	Description
Reset(1)						
106	por	-	O	VDD33	Pullup	power on reset
Mode(2)						
36	mode[0]	-	I	VDD33	Pulldown[5]	boot mode select input
35	mode[1]	-	I	VDD33	Pulldown[5]	boot mode select input
Clock(2)						
11	extal	-	I	VDD33	-	12MHz Oscillator clock in
10	xtal	-	O	VDD33	-	12MHz Oscillator clock output
I2C Interface(6)						
96	scl	GINT[18]	I/O	VDD33	Pullup	I2C clock
97	sda	GINT[19]	I/O	VDD33	Pullup	I2C data
12	scl2	GINT[86]	I/O	VDD33	Pullup	I2C clock
13	sda2	GINT[87]	I/O	VDD33	Pullup	I2C data
32	scl3	-	I/O	VDD33	Pullup	I2C clock
31	sda3	-	I/O	VDD33	Pullup	I2C data
USB OTG(5)						
111	dp	-	I/O	VCCA	-	USB data
112	dm	-	I/O	VCCA	-	USB data
108	USBDET	-	I/O	VDD33	Pulldown[5]	USB connected detect pin
116	OTG_ID	-	I/O	VCCA	-	USB mini-receptacle identifier.
115	OTG_VBUS	-	I/O	VBUS	-	USB 5V power supply pin for USB OTG
Serial Periheral Interface(SPI)(24)/SCI(2)/PWMT(4)						
119	ss1	pwm[4]/GINT[10]	I/O	VDD33	Pullup	SPI chip select
121	sck1	pwm[5]/GINT[8]	I/O	VDD33	Pullup	SPI clock
120	mosi1	pwm[6]/GINT[9]	I/O	VDD33	Pullup	SPI master output/slave input data
118	miso1	pwm[7]/GINT[11]	I/O	VDD33	Pullup	SPI master input/slave output data

Pin No.	Name[1]	Alternate	Dir.	Power	Default Pull[2,3]	Description
77	ss2	pwmt[0]]/GINT[72]	I/O	VDD33	Pullup	SPI chip select / pwm output
80	sck2	pwmt[1]]/GINT[73]	I/O	VDD33	Pullup	SPI clock / pwmt output
78	mosi2	pwmt[2]]/GINT[75]	I/O	VDD33	Pullup	SPI master output/slave input data / pwmt output
79	miso2	pwmt[3]]/GINT[74]	I/O	VDD33	Pullup	SPI master input/slave output data /pwmt output
68	ss3	GINT[76]	I/O	VDD33	Pullup	SPI chip select
67	sck3	GINT[77]	I/O	VDD33	Pullup	SPI clock
66	mosi3	sci3_rts /GINT[79]	I/O	VDD33	Pullup	SPI master output/slave input data /slave input data
65	miso3	sci3_cts /GINT[78]	I/O	VDD33	Pullup	SPI master input/slave output data slave output data
59	ss_spi4	GINT[88]	I/O	VDD33	Pullup	SPI chip select
63	sck_spi4	GINT[89]	I/O	VDD33	Pullup	SPI clock
62	spi4[0]	GINT[90]	I/O	VDD33	Pullup	SPI data bus
60	spi4[1]	GINT[91]	I/O	VDD33	Pullup	SPI data bus
58	spi4[2]	GINT[92]	I/O	VDD33	Pullup	SPI data bus
64	spi4[3]	GINT[93]	I/O	VDD33	Pullup	SPI data bus
74	ss_spi5	GINT[96]	I/O	VDD33	Pullup	SPI chip select
75	sck_spi5	GNT[97]	I/O	VDD33	Pullup	SPI clock
71	spi5[0]	GINT[98]	I/O	VDD33	Pullup	SPI data bus
73	spi5[1]	GINT[99]	I/O	VDD33	Pullup	SPI data bus
72	spi5[2]	GINT[100]	I/O	VDD33	Pullup	SPI data bus
76	spi5[3]	GINT[101]	I/O	VDD33	Pullup	SPI data bus
SD Host/MAC(9)						
86	sdh_dat[0]	phy_tx[0]/ GINT[131]	I/O	VDD33	Pullup	SD host data/MAC transmitting data pin
84	sdh_dat[1]	phy_tx[1]/ GINT[132]	I/O	VDD33	Pullup	SD host data/MAC transmitting data pin
89	sdh_dat[2]	phy_rx[0]/ GINT[133]	I/O	VDD33	Pullup	SD host data/MAC receiving data pin
91	sdh_dat[3]	phy_rx[1]/ GINT[134]	I/O	VDD33	Pullup	SD host data/MAC receiving data pin
85	sdh_cmd	rmii_mdc/ GINT[128]	I/O	VDD33	Pullup	SD host command/MAC phy config clock

Pin No.	Name[1]	Alternate	Dir.	Power	Default Pull[2,3]	Description
92	sdh_clk	rmii_clk/GINT[119]	I/O	VDD33	Pullup	SD host clock/MAC refrence clock
83	sdh_det	rmii_mdio/GINT[129]	I/O	VDD33	Pullup	SD host detect/MAC phy config io
88	sdh_wprt	phy_txen/GINT[130]	I/O	VDD33	Pullup	SD host write protect/MAC transmitting enable
90	sdh_cardint	phy_rxdv/GINT[135]	I/O	VDD33	Pullup	SD host card interrupt/MAC receiving data valid
SCI(8)/CAN(2)/PWMT(4)						
7	txd[4]	GINT[80]	I/O	VDD33	Pullup	UART transmitting data
4	rxd[4]	GINT[81]	I/O	VDD33	Pullup	UART receiving data
98	txd2	pwmt_n[0]/GINT[16]	I/O	VDD33	Pullup	UART transmitting data
99	rxd2	pwmt_n[1]/GINT[17]	I/O	VDD33	Pullup	UART receiving data
9	txd3[4]	pwmt_n[2]/GINT[82]	I/O	VDD33	Pullup	UART transmitting data/ pwm output
6	rxd3[4]	pwmt_n[3]/GINT[83]	I/O	VDD33	Pullup	UART receiving data/ pwm output
5	txd4[4]	can_tx/GINT[84]	I/O	VDD33	Pullup	UART transmitting data/CAN transmitting data
8	rxd4[4]	can_rx/GINT[85]	I/O	VDD33	Pullup	UART receiving data/CAN recerving data
Others(6)						
109	WAKE UP	-	I	VCC5V	Pulldown[5]	wake up pin
123	dac_out	-	O	VDD33	-	dac channel output
127	adc_in[0]	-	I	VDD33	-	adc channel input
81	test	-	O	VDD33	-	chip test
101	PAD_XTALO	-	O	PAD_AVDD_BBAT	-	32.768KHz oscillator clock input
100	PAD_XTALI	-	I	PAD_AVDD_BBAT	-	32.768KHz oscillator clock output
DCMI Interface (12)						
33	sensor_clkin	GINT[115]	I/O	VDD33	-	DCMI clock input
27	dcmi_pclk	GINT[113]	I/O	VDD33	Pullup	DCMI clock

Pin No.	Name[1]	Alternate	Dir.	Power	Default Pull[2,3]	Description
22	dcmi_hsync	GINT[112]	I/O	VDD33	Pullup	DCMI horizontal synchronization
21	dcmi_vsync	GINT[114]	I/O	VDD33	Pullup	DCMI vertical synchronization
30	dcmi_data[0]	GINT[104]	I/O	VDD33	Pullup	DCMI data bus
29	dcmi_data[1]	GINT[105]	I/O	VDD33	Pullup	DCMI data bus
25	dcmi_data[2]	GINT[106]	I/O	VDD33	Pullup	DCMI data bus
24	dcmi_data[3]	GINT[107]	I/O	VDD33	Pullup	DCMI data bus
23	dcmi_data[4]	GINT[108]	I/O	VDD33	Pullup	DCMI data bus
19	dcmi_data[5]	GINT[109]	I/O	VDD33	Pullup	DCMI data bus
18	dcmi_data[6]	GINT[110]	I/O	VDD33	Pullup	DCMI data bus
17	dcmi_data[7]	GINT[111]	I/O	VDD33	Pullup	DCMI data bus
LCD(20)						
55	lcd_dat[0]	mculcd_data[0]/GINT[120]	I/O	VDD33	Pullup	lcd data
57	lcd_dat[1]	mculcd_data[1]/GINT[121]	I/O	VDD33	Pullup	lcd data
56	lcd_dat[2]	mculcd_data[2]/GINT[122]	I/O	VDD33	Pullup	lcd data
41	lcd_dat[3]	mculcd_data[3]/GINT[123]	I/O	VDD33	Pullup	lcd data
40	lcd_dat[4]	mculcd_data[7]/GINT[124]	I/O	VDD33	Pullup	lcd data
38	lcd_dat[5]	mculcd_data[4]/GINT[125]	I/O	VDD33	Pullup	lcd data
37	lcd_dat[6]	mculcd_data[8]/GINT[126]	I/O	VDD33	Pullup	lcd data
44	lcd_dat[7]	mculcd_data[9]/GINT[127]	I/O	VDD33	Pullup	lcd data
54	lcd_dat[8]	mculcd_data[10]/GINT[24]	I/O	VDD33	Pullup	lcd data

Pin No.	Name[1]	Alternate	Dir.	Power	Default Pull[2,3]	Description
51	lcd_dat[9]	mculcd_data[6]/GINT[25]	I/O	VDD33	Pullup	lcd data
42	lcd_dat[10]	mculcd_data[5]/GINT[26]	I/O	VDD33	Pullup	lcd data
43	lcd_dat[11]	mculcd_data[11]/GINT[27]	I/O	VDD33	Pullup	lcd data
45	lcd_dat[12]	mculcd_data[14]/GINT[28]	I/O	VDD33	Pullup	lcd data
50	lcd_dat[13]	mculcd_data[13]/GINT[29]	I/O	VDD33	Pullup	lcd data
49	lcd_dat[14]	mculcd_data[12]/GINT[30]	I/O	VDD33	Pullup	lcd data
48	lcd_dat[15]	mculcd_data[15]/GINT[31]	I/O	VDD33	Pullup	lcd data
46	lcd_clcp	mculcd_oe_n/GINT[95]	I/O	VDD33	Pullup	lcd control signal
47	lcd_clac	mculcd_addr/GINT[94]	I/O	VDD33	Pullup	lcd control signal
52	lcd_cllp	mculcd_we_n/GINT[103]	I/O	VDD33	Pullup	lcd control signal
53	lcd_clfp	mculcd_cs_n/GINT[102]	I/O	VDD33	Pullup	lcd control signal
EPORT(4)						
15	gint[14]	SWDtio/PWM[2]	I/O	VDD33	Pullup	STExternal interrupt
16	gint[15]	SWDtclk/PWM[3]	I/O	VDD33	Pullup	STExternal interrupt
70	gint[12]	PWM[0]	I/O	VDD33	Pullup	STExternal interrupt
69	gint[13]	SWDswv/PWM[1]	I/O	VDD33	Pullup	STExternal interrupt
Power Supply(11)						

Pin No.	Name[1]	Alternate	Dir.	Power	Default Pull[2,3]	Description
3	MIPIPHY_AVDD	-	-	-	-	3.3V power input for MIPI
122	AVDD_MCC_DAC/VREFH	-	-	-	-	3.3V power input for DAC
126	AVDD_MCC_ADC/VREFH	-	-	-	-	3.3V power input for ADC
1/2/28/61 82/87/93/94/105 /117/125/	VDD33	-	-	-	-	3.3V power output
104/113	VDD_PD	-	-	-	-	1.1V power output
114	VDDA	-	-	-	-	1.1V power output
103	VDD18	-	-	-	-	1.8V power output
14/20/26/34/39	VDD33_FMC_DATA	-	-	-	-	3.3V power input for SDRAM DATA
107	VCC5V	-	-	-	-	3.3V power input for chip
110/124	VSS/VREFL	-	-	-	-	Ground
102	PAD_AVDD_BBAT	-	-	-	-	3.3V power input for PCI
95	AVDD_TSI					3.3V power for TSI

NOTES:

1. Shaded signals are for optional bond-out for more pin count package.
2. All pullups are disconnected when the signal is programmed as an output.
3. All Not-Single-Chip I/O pins will be put into input mode and be connected to pullups.
4. Pins are designed for anti-leakage.
5. Default Pull is configured by Wakeup PAD Control Register of CPM module.

Signal Description

Section 4 Package information

4.1 General

This section provides parameters for below items:

• Package Outline Dimension (POD) of package for LQFP128

4.2 POD of Package LQFP128

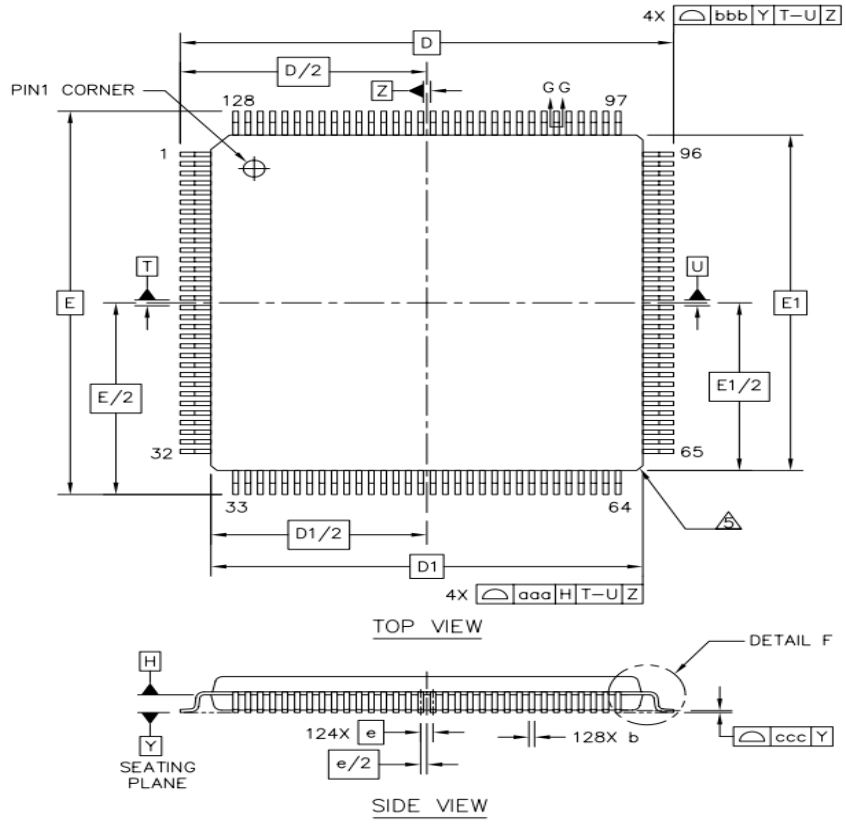

Figure 4-1 POD of Package LQFP128

Table 4-1 POD Parameters of Package LQFP128

		SYMBO	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.16	0.23
LEAD WIDTH		b1	0.13	---	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
	X	D	16 BSC		
	Y	E	16 BSC		
BODY SIZE	X	D1	14 BSC		
	Y	E1	14 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

Section 5 Part numbering

5.1 BR32F4x Series Chips Naming rules

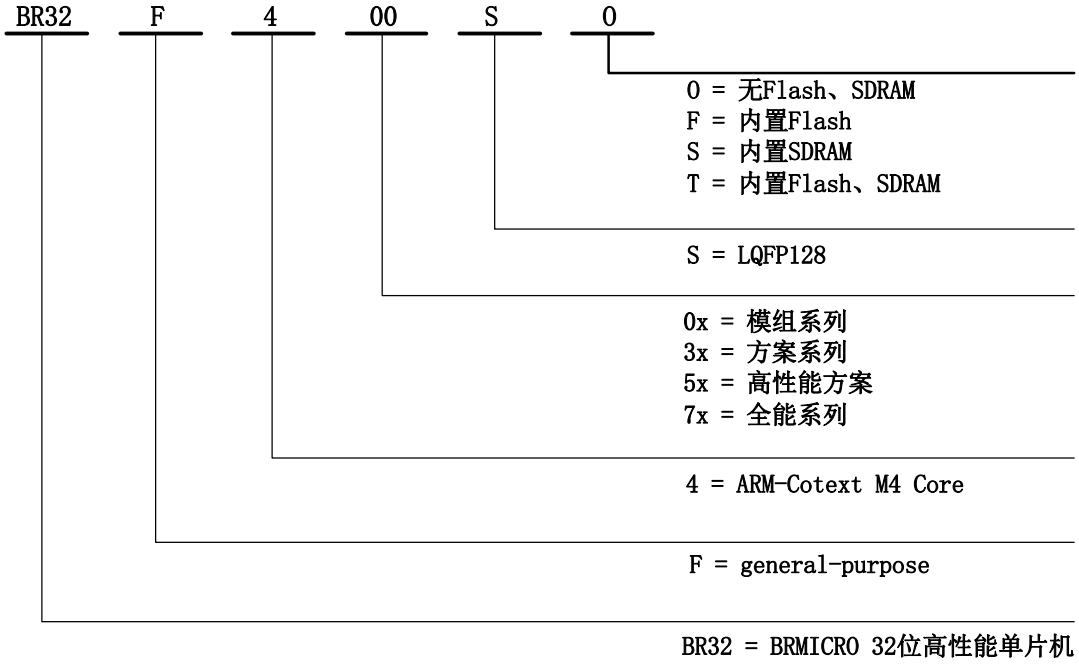

Figure 5-1 Naming rules

Part numbering

Appendix A Preliminary Electrical Characteristic

A.1 General

This section provides electrical parametrics and electrical ratings for the microcontroller unit.

A.2 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which the Chip can be exposed without permanently damaging it. See **Table A-1**.

The Chip contains circuitry to protect the inputs against damage from high static voltages; however, do not apply voltages higher than those shown in the table. Connect unused inputs to the appropriate voltage level, V_{DDH}. This device is not guaranteed to operate properly at the maximum ratings. Refer to **A.4**, **A.4**,**Table A-3**,**Table A-4** for guaranteed operating conditions.

Table A-1 Absolute Maximum Ratings

Num	Rating	Symbol	Value	Unit
1	Operating temperature range	T_{OPT}	-25 to +85	^{O}C
2	Storage temperature range	T_{STG}	-40 to +125	^{O}C

A.3 Electrostatic Discharge (ESD) Protection

Table A-2 ESD Protection Characteristics

Parameter[1,2,3,4,5]	Symbol	Value	Units
ESD target for human body model	HBM	2000	V
Latch Up	Latch UP	200	mA

NOTES:

1. This report will be invalid if reproduced in whole or in part.
2. This report refers only to the specimen(s) submitted to test, and is invalid if used separately.
3. This report is ONLY valid with the examination seal and signature of this institute.
4. The tested specimen(s) will only be preserved for thirty days from the date issued, if not collected by the applicant.
5. The failure criteria of all ESD tests should be based on the result of parametric and functional testing conducted by the customer, which follows the statement of international standards. Thus, the judgment of the curve traces provided in this report is for reference ONLY.

A.4 DC Electrical Specifications

Table A-3 DC Electrical Specificatios(3.3V)

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	V_{DDH}	3	3.3	3.6	V
Input High Voltage	V_{IH}	2	—	DVDD	V
Input Low Voltage	V_{IL}	VSS	—	0.8	V
Output High Voltage	V_{OH}	2.4	—	DVDD	V
Output Low Voltage	V_{OL}	VSS	—	0.4	V
Pull-up Resistor current	R_{PU}	50	—	—	υA
Input Leakage Current@DVDD=max,VPAD-0 o DVDD	I_{IN}	-1.2	—	1.2	υA
Fail leakagecurrent @DVDD=0,VPAD=DVDD=max	I_{PAD}	—	—	1.2	υA
Off_state leakage current@DVDD=max,VPAD=0 or DVDD	I_{OZ}	—	—	1.2	uA

A.5 Power Consumption

Table A-4 power consumption[1]

Parameter	power consumption	
	400MHz	**500MHz**
CPU run	80mA	120mA
CPU and peripherals run[1]	130mA	170mA
CPU and SDRAM run[2]	97mA	136mA
CPU,SDRAM and peripherals run	134mA	180mA
LOWPOWER MODE[3]	5mA	
POWEROFF1.0 MODE[4]	10uA	
POWEROFF2.0 MODE[5]	180nA	

NOTES:

1. All the peripherals are operated in fastest speed.
2. CPU:SDRAM=4:1 in speed.
3. Chip poweron and clock stop.

wakeup source: USI,I2C,EPORT,USB RESUME,TSI TOUCH,TIME COUNTER, RTC,WK PAD,USBDET,POR,PCI

4. Only TSI run in poweroff 1.0 mode.

wakeup source: EPORT0,TSI TOUCH,RTC,WK PAD,USBDET,POR,PCI

5. Only PCI poweron.

wakeup source: WK PAD,USBDET,POR

NOTES:

1. All the data are typical results.

A.6 AC Timing

A.6.1 SPI Interface

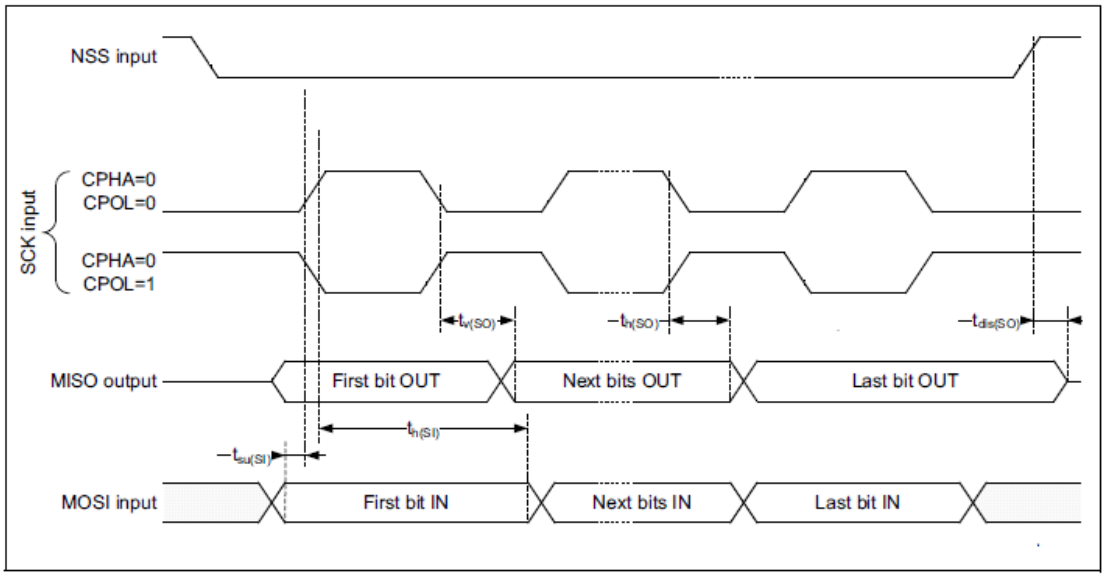

Figure A-1 SPI timing diagram

Table A-5 SPI characteristics

Symbol	Parameter	condition	min	typ	max	Unit
f_{sck}	SPI clock frequency	VCC3.3V,VDD 1.1V	-	-	50	MHz
		VCC3.3V,VDD 1.23V	-	-	62.5	
$t_{su(SI)}$	Data input setup time	VCC3.3V,VDD1.1V	-	3.9	6.9	ns
$t_{h(SI)}$	Data input hold time	VCC3.3V,VDD1.1V	-1	0	-	
$t_{dis(SO)}$	Data output disable time	VCC3.3V,VDD1.1V	5.9	8	11.9	
$t_{v(SO)}$	Data output valid time	VCC3.3V,VDD1.1V	-	9.8	14.95	
$t_{h(SO)}$	Data output hold time	VCC3.3V,VDD1.1V	2.3	3.9	-	

A.6.2 SSI(QSPI) Interface

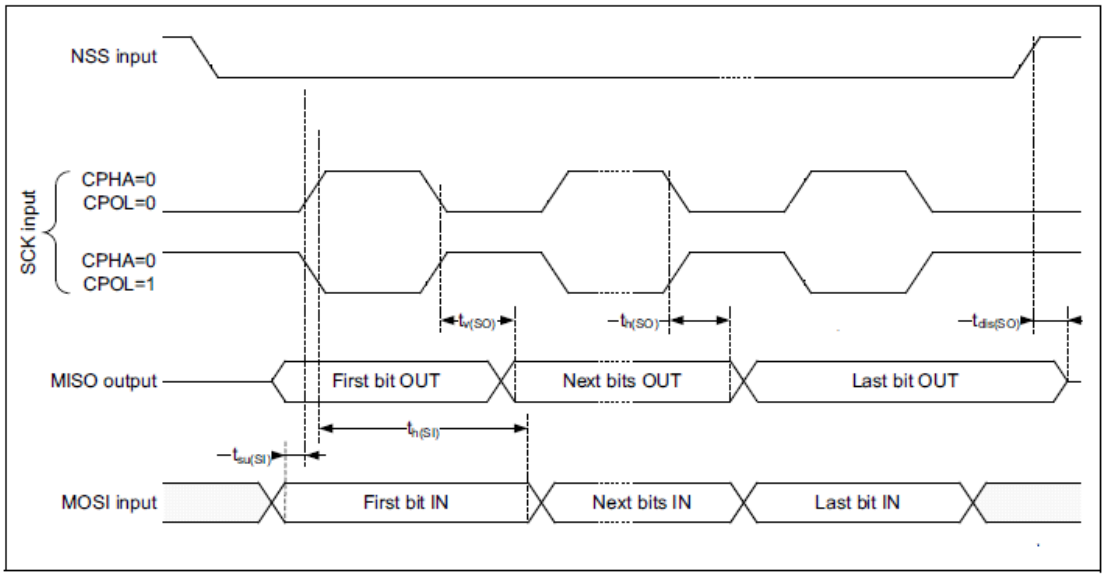

Figure A-2 SSI(QSPI) timing diagram

Table A-6 SSI(QSPI) characteristics

Symbol	Parameter	condition	min	typ	max	Unit
f_{sck}	SSI clock frequency	VCC3.3V,VDD 1.1V	-	-	100	MHz
		VCC3.3V,VDD 1.23V	-	-	125	
$t_{su(SI)}$	Data input setup time	VCC3.3V,VDD1.1V	2	-	-	ns
$t_{h(SI)}$	Data input hold time	VCC3.3V,VDD1.1V	3	-	-	
$t_{dis(SO)}$	Data output disable time	VCC3.3V,VDD1.1V	-	-	7	
$t_{v(SO)}$	Data output valid time	VCC3.3V,VDD1.1V	-	-	6	
$t_{h(SO)}$	Data output hold time	VCC3.3V,VDD1.1V	0	-	-	

A.6.3 SDRAM Interface

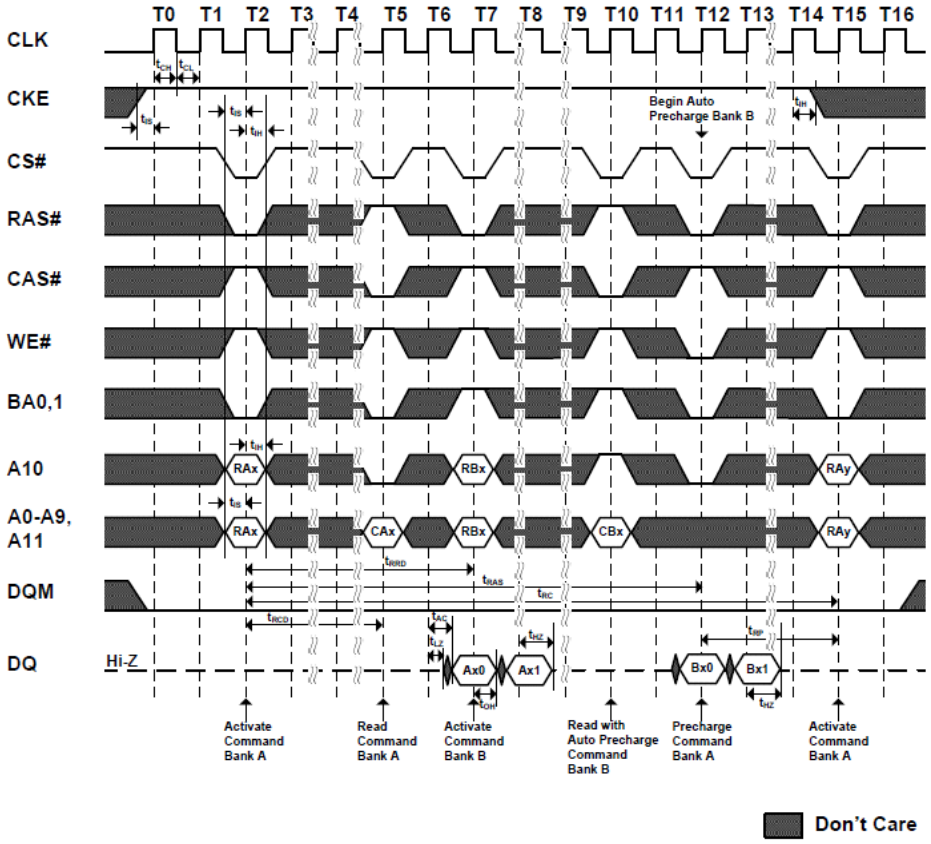

Figure A-3 Read Timing diagram (Burst Length =2,CAS# Latency=2)

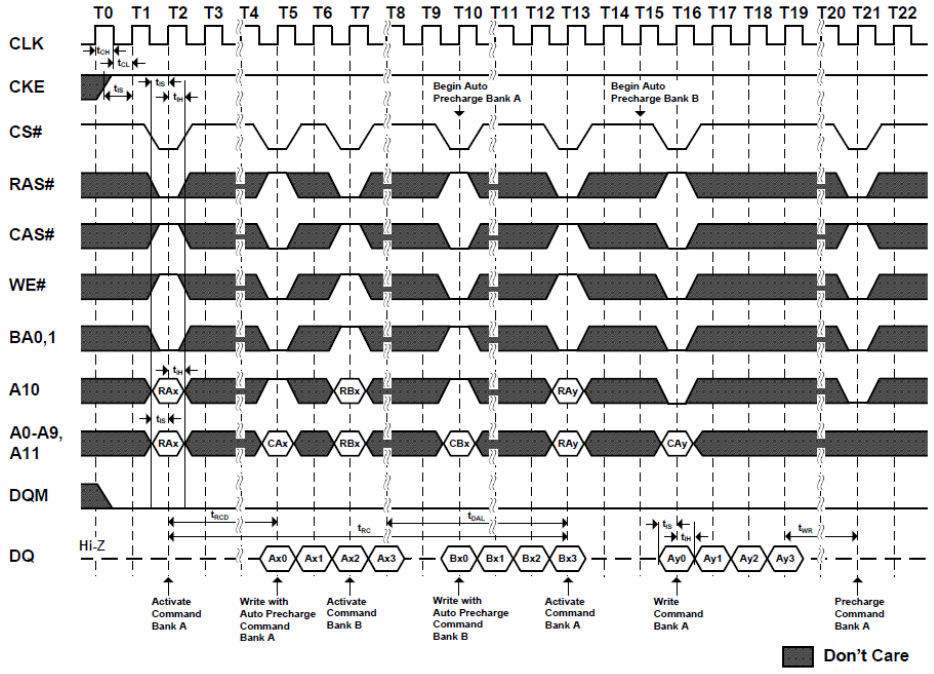

Figure A-4 Write Timing diagram (Burst Length =4)

Table A-7 SDRAM characteristics

Symbol	Parameter	condition	min	typ	max	Unit
f_{sck}	SDRAM clock frequency	VCC3.3V,VDD 1.1V	-	-	100	MHz
		VCC3.3V,VDD 1.23V	-	-	125	
t_{IS}	Data/Address/Control input setup time	VCC3.3V,VDD1.1V	1.5	-	-	ns
t_{Ih}	Data/Address/Control input hold time	VCC3.3V,VDD1.1V	0.8	-	-	
t_{OH}	Data output hold time	VCC3.3V,VDD1.1V	0	-	-	