

**BR32F450SS**

**Biometrics MCU**  
**Face & Palm vein & Finger**

**DataSheet**

**Rev2.3.2**

**CMOS**  
**Microcontroller Unit**

| <b>Release Number</b> | <b>Date</b> | <b>Author</b> | <b>Summary of Changes</b>  |
|-----------------------|-------------|---------------|--|
| 2.0.0                 | 2020/07/08  | BRMICRO       | This version is for initial version  |
| 2.1.0                 | 2020/08//11 | BRMICRO       | Adding timing  |
| 2.1.1                 | 2020/09/04  | BRMICRO       | Adjust the format  |
| 2.1.2                 | 2020/10/23  | BRMICRO       | Adding Package information   |
| 2.1.3                 | 2020/11/16  | BRMICRO       | Adding GINT PIN  |
| 2.1.4                 | 2021/02/18  | BRMICRO       | Adjust IIC3 Alternate  |
| 2.1.5                 | 2021/02/20  | BRMICRO       | For BR32F450SS   |
| 2.1.6                 | 2021/02/22  | BRMICRO       | Adjust the format  |
| 2.1.7                 | 2021/04/15  | BRMICRO       | Increase pin pull up and down  |
| 2.1.8                 | 2021/07/24  | BRMICRO       | Error content modification   |
| 2.1.9                 | 2022/03/04  | BRMICRO       | Adjust the format  |
| 2.2.0                 | 2022/06/07  | BRMICRO       | Adding application field,DMA2D,PCI   |
| 2.3.0                 | 2022/06/15  | BRMICRO       | Modify the frequency   |
| 2.3.1                 | 2022/09/23  | BRMICRO       | Add I/O DC parameters and adjust the chip package diagram                        |
| 2.3.2                 | 2022/09/29  | BRMICRO       | Add the default level of the pin and update the pull-up and pull-down of the pin |

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## Section 1 Introduction

### 1.1 Introduction

- BR32F450SS is a biometrics MCU. It is a new 32-bit general-purpose micro controller based on the ARM<sup>®</sup> Cortex<sup>®</sup>-M4 core with best cost-performance ratio in terms of enhanced processing capacity, reduced power consumption and peripheral set. This chip is operating at 400MHz frequency.
- The core features a Floating Point Unit (FPU) that accelerates single precision floating point math operations and supports all Arm single precision instructions and data types.
- It implements a full set of DSP instructions to address digital signal control markets that demand an efficient, easy-to-use blend of control and signal processing capabilities. It also provides a Memory Protection Unit (MPU) and powerful trace technology for enhanced application security and advanced debug support.
- Multiple accelerator are embedded inside the chip to deal with diverse scenarios: face recognition accelerator, palm vein recognition accelerator , fingerprint recognition accelerator and 2-D barcode Accelerator.
- The temperature range is of -25°C to 65°C.
- Chip package is:

LQFP128

### 1.2 Application Field

- The above features make BR32F450SS devices suitable for a wide range of interconnection and advanced applications, especially in areas such as industrial control, identification under the real name system, human machine interface, attendance, security and alarm systems, graphic display, access control, 2-D barcode decoding and so on.

### 1.3 Features

- Cache
  - On-chip, 32K Bytes ICache, 32K Bytes DCache.
  - Has two AHB bus interfaces, a master and a slave interface.

## Introduction

- Has a 2-way set-associative organization.
- Has an AHB bus interface to access its programmer's model.
- Support for debug
- Integrated 8M Byte of Synchronous Dynamic Random-Access Memory(SDRAM)
- On-chip, 64K Bytes of static random-access memory can only be accessed by CPU(TCMSRAM)
- On-chip, 128K Bytes of static random-access memory (SRAM):
  - Single cycle byte, half-word (16-bit), and word (32-bit) reads and writes
- On-chip, 64K Bytes of static read only memory (ROM):
  - Single cycle byte, half-word (16-bit), and word (32-bit) read access.
- On-chip embedded flash (EFLASH)
  - Memory Organization: 256K Bytes LP
  - Read of bytes, aligned halfwords (16 bits) and aligned words (32 bits)
  - Automated program and erase operation
  - Optional interrupt on command completion
  - Data Retention: 10 years under 85 degrees
  - 0.99~1.21V/1.5~1.98V dual power supplies
- CPM
  - Multiple system clock sources
  - Separate clock divider
  - Support for power saving mode
  - Module clock can be gated separately
- Programmable 32bit Interrupt timer(PIT) :
  - 32-bit counter with modulus "initial count" register
  - Selectable as free running or count down
- Watchdog timer(WDT) :
  - 16-bit counter with modulus "initial count" register
  - Pause option for low-power modes
- Time Counter :
  - 16-bit counter with modulus "initial count" register

- Pause option for low-power modes
- Reset :
  - Separate reset in and reset out signals
  - Five sources of reset:
    - Power-on reset
    - Software reset
    - Watchdog timer
    - Time Counter
    - Power Attack Detect Reset (Low and High Voltage Detect Reset)
  - Status flag indicates source of last reset
- DMA Controller
  - Four independently programmable DMA controller channels
  - Data transfers in 8, 16, 32, 64bits
  - Support single transfer, Burst 4, 8, 16 transfer, and burst always under a special case.
  - Support single cycle transfer
  - Support automatic transfer mode
  - Support LLI transfer mode
  - Follow a fixed priority rule
- DMA2D
  - The Chrom-Art Accelerator™ (DMA2D) is a graphic accelerator which offers advanced bit blitting, row data copy and pixel format conversion. It supports the following functions:
    - Rectangle filling with a fixed color
    - Rectangle copy
    - Rectangle copy with pixel format conversion
    - Rectangle composition with blending and pixel format conversion.
  - Various image format coding are supported, from indirect 4bpp color mode up to 32bpp direct color. It embeds dedicated memory to store color lookup tables.
  - An interrupt can be generated when an operation is complete or at a programmed watermark.



## Introduction

- All the operations are fully automatized and are running independently from the CPU or the DMAs.
- 4 operating modes: register-to-memory, memory-to-memory, memory-to-memory with pixel format conversion, and memory-to-memory with pixel format conversion and blending.
- EDMAC
  - The EDMAC is the controller which sends data from SRAM to peripheral or from peripheral to SRAM
  - Two independently programmable DMA controller channels
  - Programmable transfer total number
  - Programmable read buffer address and write buffer address
  - Multiple peripheral select
  - Support read, write and write then read transfer
- CRC coprocessor
  - Support CRC32 / CRC16 / CRC8
  - Support DMAC Data from CRC
  - Support EDMAC Data from CRC
- External interrupts supported(EPORT) :
  - Rising/falling edge select
  - Low-level sensitive
  - Ability for software generation of external interrupt event
  - Interrupt pins configurable as general-purpose I/O
- I2C Controller
  - Supports 10 bit addressing.
  - Supports Standard Mode, Fast Mode and High-Speed Mode
  - Software option to select between High-Speed mode and Standard/Fast mode
  - Compatibility with standard and fast-mode of I2C bus version 2.1 standard.
  - Multiple-master operation.
  - Software-programmable for one of 64 different serial clock frequencies.
  - Software-selectable acknowledge bit.

## Introduction

- Interrupt-driven, byte-by-byte data transfer.
- Arbitration-lost interrupt with automatic mode switching from master to slave.
- Transfer completion and read configure interrupt.
- Start and stop signal generation/detection.
- Repeated START signal generation.
- Acknowledge bit generation/detection.
- Bus-busy detection.
- Option slave address receiving enable when system clock stop mode
- SCL or SDA line gpio function supported
- Serial communications interface (SCI):
  - Full-duplex operation
  - 13-bit baud rate prescaler
  - Programmable 8-bit or 9-bit data format
  - Separately enabled transmitter and receiver
  - Separate receiver and transmitter CPU interrupt requests
  - Two receiver wakeup methods (idle line and address mark)
  - Receiver framing error detection
  - Hardware parity checking
  - 1/16 bit-time noise detection
  - General-purpose I/O capability
- Serial communications interface (SCI\_TS):
  - Separate 16x9 transmit (TX) and receive (RX) FIFOs to reduce CPU interrupt service loading
  - FIFO trigger levels of 1/8, 1/4, 1/2, 3/4, and 7/8
  - Automatic hardware flow control supported
  - Serial IR interface low-speed, IrDA-compatible (up to 115.2Kbit/s)
  - Full-duplex operation
  - 13-bit baud rate prescaler
  - Programmable 8-bit or 9-bit data format
  - Separately enabled transmitter and receiver

## Introduction

- Separate receiver and transmitter CPU interrupt requests
- Two receiver wakeup methods (idle line and address mark)
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection
- General-purpose I/O capability
- Serial peripheral interfaces (SPI) :
  - Master mode and slave mode configurable
  - Slave select output
  - Mode fault error flag with CPU interrupt capability
  - Separate transmit and receive FIFOs
  - Serial clock with programmable polarity and phase
  - Control of SPI operation during doze mode
- USBOTG 2.0
  - Supports internal reference clock or external 12MHz crystal reference clock
  - Performs all transaction scheduling in hardware
  - Operates either as a function controller for a USB peripheral or as the host/peripheral in point-to-point communications with another USB function
  - Synchronous RAM interface for FIFOs
  - Supports point-to-point communications with one high-speed device
  - Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
  - Supports Suspend and Resume
  - Configurable for up to 15 additional Transmit endpoints and up to 15 additional Receive endpoints
  - Configurable FIFOs, including the option of dynamic FIFO sizing
  - Support for DMA access to FIFOs
- Soft connect/disconnect option PWM
  - Programmable period
  - Programmable duty cycle

## Introduction

- Two Dead-Zone generator
- Capture function
- Pins can be configured as general-purpose I/O
- PWM
- 16-bit up, down, up/down auto-reload counter
- 16-bit programmable prescaler allowing dividing (also “on the fly”) the counter clock frequency either by any factor between 1 and 65536
- Up to 4 independent channels
- Complementary outputs with programmable dead-time
- Synchronization circuit to control the timer with external signals and to interconnect several timers together
- Repetition counter to update the timer registers only after a given number of cycles of the counter
- Interrupt/DMA generation on the some events
- Controller Area Network (CAN):
- Full implementation of the CAN protocol specification, version 2.0B
- Flexible Message Buffers (up to 64) of zero to eight bytes data length
- Programmable loop-back mode supporting self-test operation
- Time Stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Ethernet MAC:
- Compliant with RMII
- Include internal DMA
- Include RXFIFO and TXFIFO
- Maskable interrupts
- Automatic receiving data according to the actual length of the frame
- SD\_HOST 2.0:
- Supports Secure Digital I/O protocol commands
- Supports Command Completion signal and interrupt to host processor
- Single-channel; single engine used for Transmit and Receive, which are mutually exclusive

## Introduction

- Fully synchronous design operating on a single system clock
- Dual-buffer and chained descriptor linked list
- Programmable interrupt options for different operational conditions
- ADC
  - 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
  - ADC conversion time: 1.0  $\mu$ s for 12-bit resolution (1 MHz), 0.88  $\mu$ s conversion time for 10 bit resolution, faster conversion times can be obtained by lowering resolution.
  - Programmable sampling time
  - DMA support
- DAC
  - Left or right data alignment
  - DMA capability
  - External triggers for conversion
  - Programmable internal buffer
  - Input voltage reference, VDDA
  - FIFO Based operation
- Secure features
  - Internal power on reset
  - Voltage detector
  - Light detector
  - Power Glitch detector
  - Metal Shield protection
  - Temperature detector
  - Data encryption
  - Clock and reset pulse filtration
  - Safe optimized routing
- Crypto Accelerator module
  - Large operand size N integer arithmetic  
32 \* R bits  
R is positive integer from 1 to 64

## Introduction

- Programmable scalar or modulo operation
$$Y = (A * B) \text{ mod } M$$
$$Y = (A^E) \text{ mod } M$$
- Discrete "sea-of-gates" implementation to protection against SPA and probing attacks
- AES module
  - Support AES encryption/decryption algorithm
  - Support AES algorithm with 128/192/256 bits key
  - Support Electronic Code Book (ECB ) mode operation and CTR(counter) mode operation
- SHA coprocessor
  - SM3(256)
  - SHA-0(160)
  - SHA-1(160)
  - SHA-224(224)
  - SHA-256(256)
  - SHA-384(384)
  - SHA-512(512)
  - Share hardware between different SHA processing
- SM4 module
  - Support sm4 encryption/decryption algorithm.
  - Support sm4 algorithm with 128 bits key
  - Support ECB and CBC mode
  - Support MLBBUS Interface
- DES coprocessor
  - Support DES and Triple-DES encryption and decryption algorithm
  - Support DES algorithm with 64(56) bits key
  - Support Triple-DES algorithm with 128(112) bits or 192(168) bits key
  - Support ECB mode and CBC mode
  - Support MLBBUS Interface
- TRNG( random number generator)

## Introduction

- Max Rate: 20Mbps
- PMU\_RTC
  - Internal 32KHz oscillator
  - Load time data to and read time data from seconds, minutes, hours and days counters
  - Support alarm settings
  - Interrupt sources:second, minute, hour,day interrupts,programmable alarm interrupts ,1KHZ/32KHZ periodic interrupts .
- PXLPL
  - Single AHB master bus architecture
  - User programmable offset for sources and destination areas of picture for dma
  - User programmable sources and destination addresses on the whole memory space
  - Copy from an area to another
  - Support average filter algorithm
  - Support histogram algorithm
  - Support hough algorithm
  - Support Reed-Solomon(RS) error correction algorithm
  - Support binary image
  - Support look for Minmum value,Maxmum value and computing average value in the block(Min\_MAX\_Average, MMA),The image split number of blocks is no more than 32. Support user programmable the block size.
  - Look for Minmum value,Maxmum value and computing average value in the block(Min\_MAX\_Average, MMA), support the image data from Digital Camera Interface (DCMI) directly.
  - Support black white run length coding algorithm
  - Interrupt generation on process completion
  - Support YOLO v3 deep learning end-to-end real-time target detection algorithm
  - Darknet light open source deep learning framework realized by YOLO v3, with less dependence and good portability. Due to its outstanding ability of speed and precision, especially small object detection, Darknet is widely used at present

- LCDC
  - compliance to the *AMBA Specification (Rev 2.0)* onwards for easy integration into SoC implementation
  - dual 16-deep programmable 32-bit wide FIFOs for buffering incoming display
  - data
  - supports single and dual panel mono *Super Twisted Nematic* (STN) displays with 4 or 8-bit interfaces
  - supports single and dual-panel color and monochrome STN displays
  - supports *Thin Film Transistor* (TFT) color displays
  - resolution programmable up to 1024 x 768
  - 15 gray-level mono, 3375 color STN, and 32K color TFT support
  - 1, 2, or 4 *bits-per-pixel* (bpp) palettized displays for mono STN
  - 1, 2, 4 or 8 bpp palettized color displays for color STN and TFT
  - 16 *bits-per-pixel* (bpp) true-color non-palettized, for color STN and TFT
  - programmable timing for different display panels
  - 256 entry, 16-bit palette RAM, arranged as a 128 x 32-bit RAM physically
  - frame, line and pixel clock signals
  - AC bias signal for STN and data enable signal for TFT panels
  - patented gray scale algorithm
  - supports little and big-endian, as well as WinCE data formats.
  - supports gamma correction
  - supports rgb565 output
- DCM I
  - 8-bit parallel interface(DVP)
  - Embedded/external line and frame synchronization
  - Continuous or snapshot mode
  - Crop feature
  - Supports the following data formats:
    - 8- bit progressive video: either monochrome or raw bayer
    - YCbCr 4:2:2 progressive video and gray output



## Introduction

- YCbCr 4:2:0 directly output and gray output
- RGB 565 progressive video and gray output
- Supports internal DMA and external DMA for RGB and gray data output simultaneously
- Supports internal DMA and external DMA exchangeable
- Supports MIPI-IPI format
- Supports Crop for gray window
- SSI
  - Serial-master operation
  - DMA controller interface – Enables the SSI to interface to a DMA controller over the bus using handshaking interface for transfer requests.
  - Clock stretching support in enhanced SPI transfers
  - Data item size (4 to 32 bits) – Item size of each data transfer under control of the programmer
  - FIFO depth – Configurable depth of the transmit and receive FIFO buffers from 2 to 256 words deep. The FIFO width is fixed at 32 bits
  - Enhanced SPI support
  - Execute in Place (XIP) mode support
- PCI
  - VD detect voltage of button cell and chip output voltage.
  - NVSRAM 32x32bit
  - SDIO 8 bit detect
  - Async Timer
- GPIO
  - Support 83 GPIO

1.4 Block Diagram

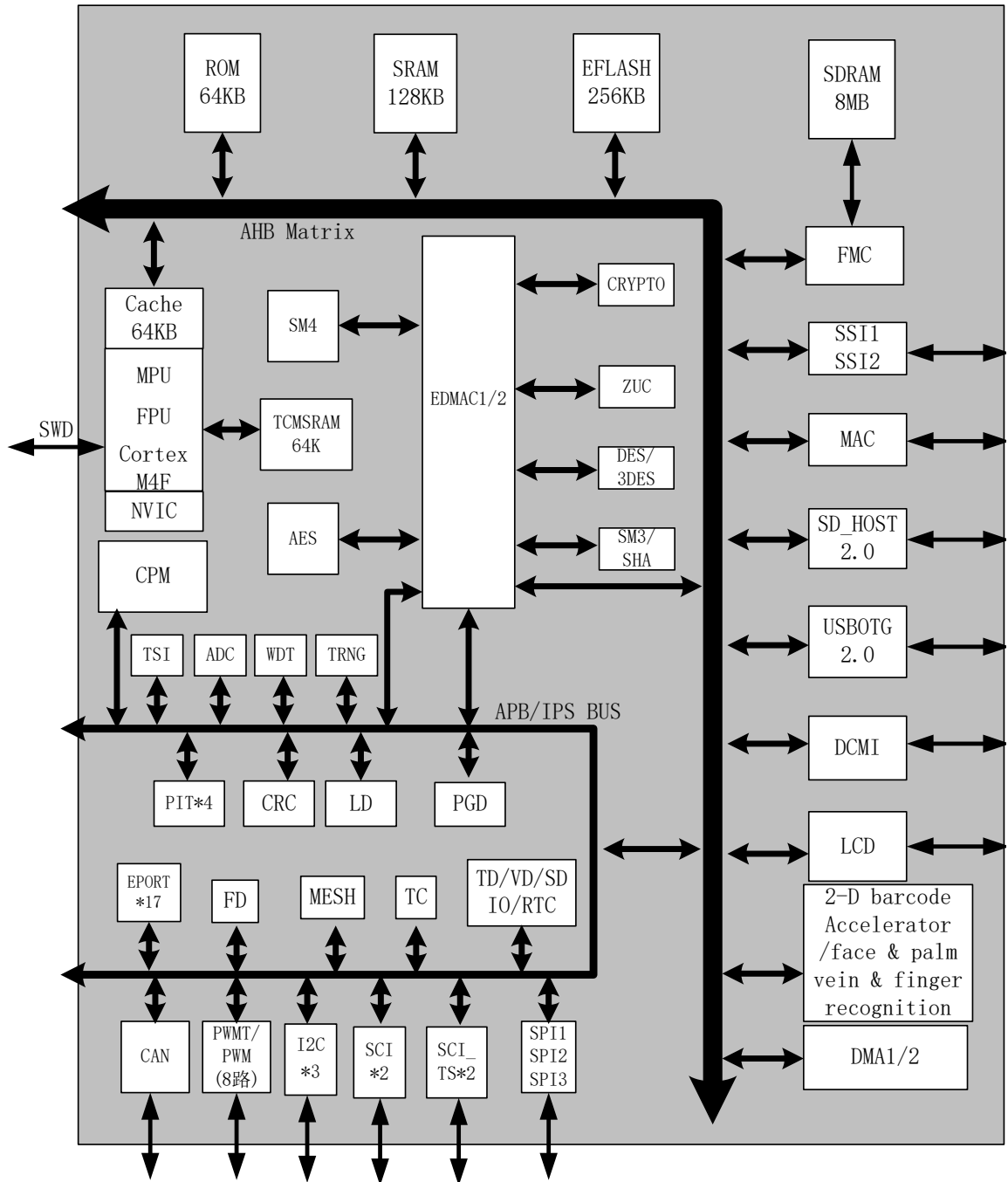


Figure 1-1 Block Diagram

## Section 2 System Memory Map

### 2.1 Introduction

The address map, shown in **2.2**, includes:

- 64K Bytes of internal read only memory (ROM)
- 128K Bytes of internal static random-access memory (SRAM)
- 64K Bytes TCMSRAM
- 256K Bytes EFLASH
- 8M Bytes SDRAM
- Internal memory mapped registers
- Memory support power failure protection

### 2.2 Address Map

**Table 2-1 Boot Modes**

| mode[1] | mode[0] | Boot mode | Aliasing                             |
|---------|---------|-----------|--------------------------------------|
| 0       | 0       | ROM       | ROM is selected as the boot space    |
| 0       | 1       | EFLASH    | EFLASH is selected as the boot space |
| 1       | 0       | SDRAM     | SDRAM is selected as the boot space  |

**Table 2-2 Memory mapping vs Boot mode/physical remap**

| Address               | Boot/Remap in ROM | Boot/Remap in EFLASH | Boot/Remap in SDRAM | Boot/Remap in SPI FLASH |
|-----------------------|-------------------|----------------------|---------------------|-------------------------|
| 0xA4000000~0xA7FFFFFF | SDRAM2LCD         | SDRAM2LCD            | SDRAM2LCD           | SDRAM2LCD               |
| 0x80000000~0x87FFFFFF | SDRAM             | SDRAM                | SDRAM               | SDRAM                   |
| 0x20000000~0x2001FFFF | SRAM              | SRAM                 | SRAM                | SRAM                    |
| 0x1FFF0000~0x1FFFFFFF | TCMSRAM           | TCMSRAM              | TCMSRAM             | TCMSRAM                 |
| 0x18000000~0x1BFFFFFF | SDRAM (Cached)    | SDRAM (Cached)       | SDRAM (Cached)      | SDRAM (Cached)          |

## System Memory Map

**Table 2-2 Memory mapping vs Boot mode/physical remap**

|                           |                        |                         |                        |                        |
|---------------------------|------------------------|-------------------------|------------------------|------------------------|
| 0x14000000~<br>0x17FFFFFF | SPI2 FLASH<br>(Cached) | SPI2 FLASH<br>(Cached)  | SPI2 FLASH<br>(Cached) | SPI2 FLASH<br>(Cached) |
| 0x10000000~<br>0x13FFFFFF | SPI1 FLASH<br>(Cached) | SPI1 FLASH<br>(Cached)  | SPI1 FLASH<br>(Cached) | SPI1 FLASH<br>(Cached) |
| 0x08000000~<br>0x0803FFFF | EFLASH                 | EFLASH                  | EFLASH                 | EFLASH                 |
| 0x04000000~<br>0x0400FFFF | ROM                    | ROM                     | ROM                    | ROM                    |
| 0x00000000~<br>0x03FFFFFF | ROM(64K)<br>Aliased    | EFLASH(256K)<br>Aliased | SDRAM(16M)<br>Aliased  | SSI1(64M)<br>Aliased   |

# System Memory Map

**Table 2-3 Register Address Location Map**

|             |        |          |                           |
|-------------|--------|----------|---------------------------|
| 0x4000_0000 | 4Kbyte | AHB_IPS1 | IO Control Module(IOCTRL) |
| 0x4000_1000 | 4Kbyte |          | Chip configuration (CCM)  |
| 0x4000_2000 | 4Kbyte |          | Reset (RESET)             |
| 0x4000_3000 | 4Kbyte |          | TFM                       |
| 0x4000_4000 | 4Kbyte |          | CPM                       |
| 0x4000_5000 | 4Kbyte |          | Watchdog timer (WDT)      |
| 0x4000_6000 | 4Kbyte |          | TC                        |
| 0x4000_7000 | 4Kbyte |          | PIT1                      |
| 0x4000_8000 | 4Kbyte |          | PIT2                      |
| 0x4000_9000 | 4Kbyte |          | Edge Port 16(EPORT16)     |
| 0x4000_a000 | 4Kbyte |          | EDMAC1                    |
| 0x4000_b000 | 4Kbyte |          | Edge Port 14(EPORT14)     |
| 0x4000_c000 | 4Kbyte |          | Edge Port 15(EPORT15)     |
| 0x4000_d000 | 4Kbyte |          | PIT3                      |
| 0x4000_e000 | 4Kbyte |          | PIT4                      |
| 0x4000_f000 | 4Kbyte |          | CAN                       |
| 0x4001_0000 | 4Kbyte |          | SPI1                      |
| 0x4001_1000 | 4Kbyte |          | SPI2                      |
| 0x4001_2000 | 4Kbyte |          | SPI3                      |
| 0x4001_3000 | 4Kbyte |          | SCI1                      |
| 0x4001_4000 | 4Kbyte |          | SCI2                      |
| 0x4001_5000 | 4Kbyte |          | Reserved                  |
| 0x4001_6000 | 4Kbyte |          | USI3                      |
| 0x4001_7000 | 4Kbyte |          | I2C                       |
| 0x4001_8000 | 4Kbyte |          | PWM                       |
| 0x4001_9000 | 4Kbyte |          | Edge Port (EPORT)         |
| 0x4001_a000 | 4Kbyte |          | Edge Port 1(EPORT1)       |
| 0x4001_b000 | 4Kbyte |          | I2C2                      |
| 0x4001_c000 | 4Kbyte |          | I2C3                      |
| 0x4001_d000 | 4Kbyte |          | SCI_TS1                   |

# System Memory Map

|             |        |          |                                     |                                       |
|-------------|--------|----------|-------------------------------------|---------------------------------------|
| 0x4001_e000 | 4Kbyte | AHB_IPS1 | SCI_TS2                             |                                       |
| 0x4001_f000 | 4Kbyte |          | PWMT                                |                                       |
| 0x4002_0000 | 4Kbyte |          | ADC                                 |                                       |
| 0x4002_1000 | 4Kbyte |          | DAC                                 |                                       |
| 0x4002_2000 | 4Kbyte |          | MCC                                 |                                       |
| 0x4002_3000 | 4Kbyte |          | TSI                                 |                                       |
| 0x4002_4000 | 4Kbyte |          | Edge Port 2(EPORT2)                 |                                       |
| 0x4002_5000 | 4Kbyte |          | Edge Port 3(EPORT3)                 |                                       |
| 0x4002_6000 | 4Kbyte |          | Edge Port 4(EPORT4)                 |                                       |
| 0x4002_7000 | 4Kbyte |          | Edge Port 5(EPORT5)                 |                                       |
| 0x4002_8000 | 4Kbyte |          | Edge Port 6(EPORT6)                 |                                       |
| 0x4002_9000 | 4Kbyte |          | Edge Port 7(EPORT7)                 |                                       |
| 0x4002_a000 | 4Kbyte |          | Edge Port 8(EPORT8)                 |                                       |
| 0x4002_b000 | 4Kbyte |          | Edge Port 9(EPORT9)                 |                                       |
| 0x4002_c000 | 4Kbyte |          | Edge Port 10(EPORT10)               |                                       |
| 0x4002_d000 | 4Kbyte |          | Edge Port 11(EPORT11)               |                                       |
| 0x4002_e000 | 4Kbyte |          | Edge Port 12(EPORT12)               |                                       |
| 0x4002_f000 | 4Kbyte |          | Edge Port 13(EPORT13)               |                                       |
| 0x4003_0000 | 4Kbyte |          | LD                                  |                                       |
| 0x4003_1000 | 4Kbyte |          | True Random Number Generator (TRNG) |                                       |
| 0x4003_2000 | 4Kbyte |          | PGD                                 |                                       |
| 0x4003_3000 | 4Kbyte |          | SEC_DET                             |                                       |
| 0x4003_4000 | 4Kbyte |          | PCI                                 |                                       |
| 0x4003_5000 | 4Kbyte |          | PMU_RTC                             |                                       |
| 0x4003_6000 | 4Kbyte |          | Reserved                            |                                       |
| 0x4003_7000 | 4Kbyte |          | CRYPTO                              |                                       |
| 0x4003_8000 | 4Kbyte |          | SHA                                 |                                       |
| 0x4003_9000 | 4Kbyte |          | EDMAC0                              |                                       |
| 0x4003_a000 | 4Kbyte |          | Reserved                            |                                       |
| 0x4004_0000 | 4Kbyte |          | AHB1(AHB_CLB)                       | Data Encryption Standard Module (DES) |
| 0x4004_1000 | 4Kbyte |          |                                     | AES                                   |
| 0x4004_2000 | 4Kbyte |          |                                     | SM4                                   |
| 0x4004_3000 | 4Kbyte |          | ZUC                                 |                                       |
| 0x4004_4000 | 4Kbyte |          | AHB2                                | CRC0                                  |
| 0x4004_5000 | 4Kbyte | CRC1     |                                     |                                       |
| 0x4004_6000 | 4Kbyte | DMAC1    |                                     |                                       |
| 0x4004_7000 | 4Kbyte | DMAC2    |                                     |                                       |
| 0x4004_8000 | 4Kbyte | CLCD     |                                     |                                       |
| 0x4004_9000 | 4Kbyte | TRNG_OSC |                                     |                                       |
| 0x4004_a000 | 4Kbyte | SD_HOST  |                                     |                                       |

## System Memory Map

|             |         |               |               |      |
|-------------|---------|---------------|---------------|------|
| 0x4004_c000 | 4Kbyte  | AHB3          | USBC          |      |
| 0x4005_0000 | 4Kbyte  | AHB_APB       | MIPI          |      |
| 0x4005_1000 | 4Kbyte  |               | Cache_Config  |      |
| 0x4005_2000 | 4Kbyte  |               | DMA2D         |      |
| 0x4005_3000 | 4Kbyte  |               | DCMI          |      |
| 0x4005_4000 | 4Kbyte  |               | PXLP          |      |
| 0x4005_5000 | 4Kbyte  |               | Cache2_Config |      |
| 0x4005_6000 | 4Kbyte  |               | DCMI_DVP      |      |
| 0x4005_7000 | 4Kbyte  |               | I2S           |      |
| 0x4006_0000 | 64Kbyte |               | AHB_MAC       | MAC  |
| 0x6000_0000 | 4Kbyte  |               | AHB_SSI1      | SSI1 |
| 0x7000_0000 | 4Kbyte  | AHB_SSI2      | SSI2          |      |
| 0x9c00_0000 | 4Kbyte  | AHB_SDRAM     | SDRAM         |      |
| 0xa800_0000 | 4Kbyte  | AHB_SDRAM2LCD | SDRAM2LCD     |      |
| 0xe000_0000 | 4Kbyte  | M4            | M4 SYS        |      |

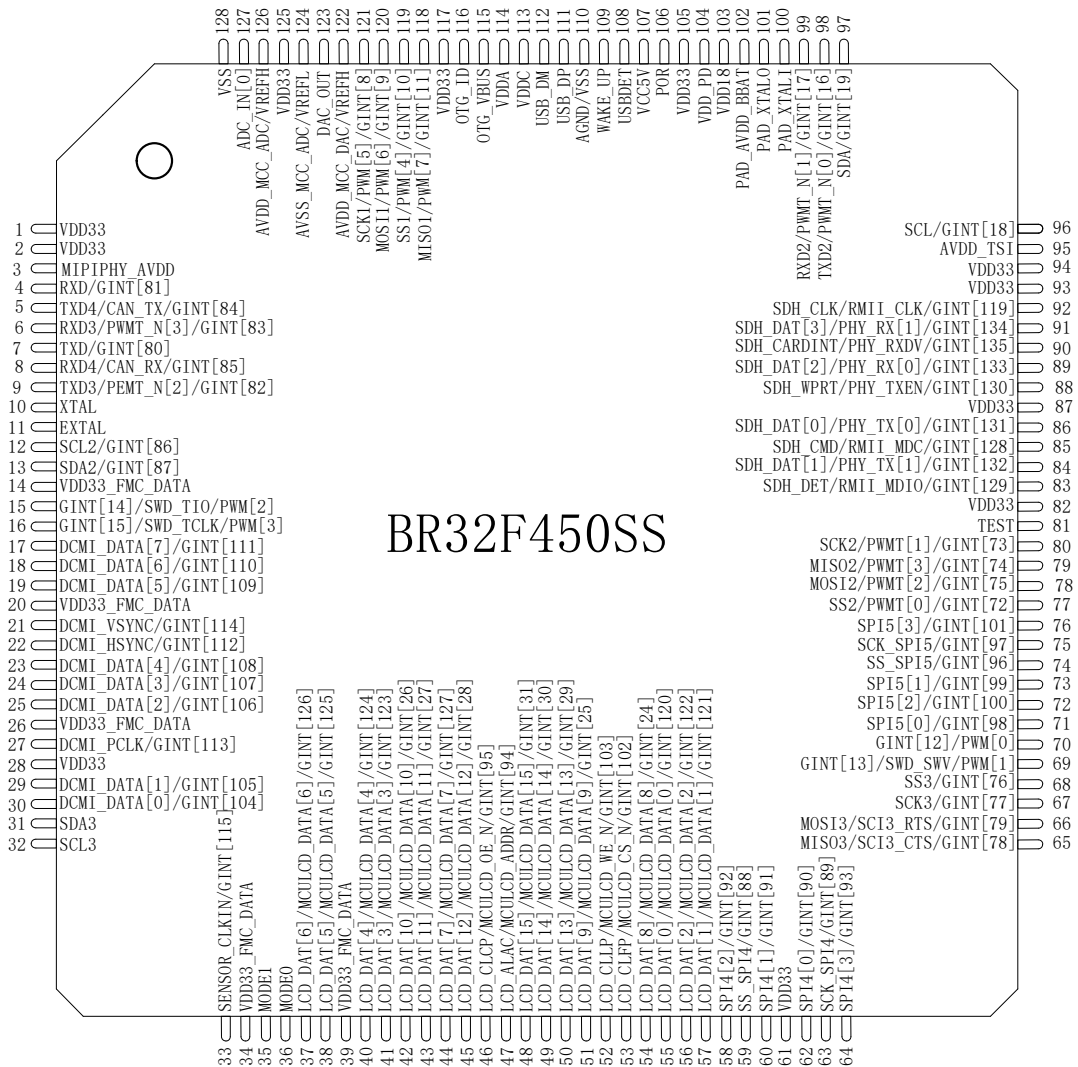
## Section 3 Signal Description

### 3.1 Introduction

The chip is available in package:

- LQFP128 (including 8MB SDRAM )

### 3.2 Package Pinout Summary





# Signal Description

## 3.3 Signal Properties Summary

below is the signal description.

**Table 3-1 Signal Description**

| Pin No.                      | Name <sup>1</sup> | Alternate          | Dir. | Power | Default | Pin Pull              | Description                         |
|------------------------------|-------------------|--------------------|------|-------|---------|-----------------------|-------------------------------------|
| <b>Reset(1)</b>              |                   |                    |      |       |         |                       |                                     |
| 106                          | por               | -                  | I    | VDD33 | H       | -                     | power on reset                      |
| <b>Mode(2)</b>               |                   |                    |      |       |         |                       |                                     |
| 36                           | mode[0]           | -                  | I    | VDD33 | L       | -                     | boot mode select input              |
| 35                           | mode[1]           | -                  | I    | VDD33 | L       | -                     | boot mode select input              |
| <b>Clock(2)</b>              |                   |                    |      |       |         |                       |                                     |
| 11                           | extal             | -                  | I    | VDD33 | -       | -                     | 12MHz Oscillator clock in           |
| 10                           | xtal              | -                  | O    | VDD33 | -       | -                     | 12MHz Oscillator clock output       |
| <b>USB OTG(5)</b>            |                   |                    |      |       |         |                       |                                     |
| 111                          | dp                | -                  | I/O  | VCCA  | -       | -                     | USB data                            |
| 112                          | dm                | -                  | I/O  | VCCA  | -       | -                     | USB data                            |
| 108                          | USBDET            | -                  | I/O  | VDD33 | -       | Pulldown <sup>3</sup> | USB connected detect pin            |
| 116                          | OTG_ID            | -                  | I/O  | VCCA  | -       | -                     | USB mini-receptacle identifier.     |
| 115                          | OTG_VBUS          | -                  | I/O  | VBUS  | -       | -                     | USB 5V power supply pin for USB OTG |
| <b>EPORT(4)</b>              |                   |                    |      |       |         |                       |                                     |
| 15                           | gint[14]          | SWD_TIO/PWM[2]     | I/O  | VDD33 | H       | Pullup/Pulldown       | STExternal interrupt                |
| 16                           | gint[15]          | SWD_TCLK/PWM[3]    | I/O  | VDD33 | H       | Pullup/Pulldown       | STExternal interrupt                |
| 70                           | gint[12]          | PWM[0]             | I/O  | VDD33 | H       | Pullup/Pulldown       | STExternal interrupt                |
| 69                           | gint[13]          | SWD_SWV/PWM[1]     | I/O  | VDD33 | H       | Pullup/Pulldown       | STExternal interrupt                |
| <b>SCI(8)/CAN(2)/PWMT(4)</b> |                   |                    |      |       |         |                       |                                     |
| 7                            | txd <sup>2</sup>  | GINT[80]           | I/O  | VDD33 | H       | Pullup                | UART transmitting data              |
| 4                            | rx <sup>4</sup>   | GINT[81]           | I/O  | VDD33 | H       | Pullup                | UART receiving data                 |
| 98                           | txd <sup>2</sup>  | PWMT_N[0]/GINT[16] | I/O  | VDD33 | H       | Pullup/Pulldown       | UART transmitting data              |
| 99                           | rx <sup>2</sup>   | PWMT_N[1]/GINT[17] | I/O  | VDD33 | H       | Pullup/Pulldown       | UART receiving data                 |
| 9                            | txd <sup>3</sup>  | PWMT_N[2]/GINT[82] | I/O  | VDD33 | H       | Pullup                | UART transmitting data /pwm output  |

## Signal Description

| Pin No.  | Name <sup>1</sup>             | Alternate          | Dir. | Power | Default | Pin Pull        | Description                                      |
|--|-------------------------------|--------------------|------|-------|---------|-----------------|--|
| 6  | rx <sub>d3</sub> <sup>4</sup> | PWMT_N[3]/GINT[83] | I/O  | VDD33 | H       | Pullup          | UART receiving data /pwm output                  |
| 5  | tx <sub>d4</sub> <sup>4</sup> | CAN_TX/GINT[84]    | I/O  | VDD33 | H       | Pullup          | UART transmitting data /CAN transmitting data    |
| 8  | rx <sub>d4</sub> <sup>4</sup> | CAN_RX/GINT[85]    | I/O  | VDD33 | H       | Pullup          | UART receiving data /CAN receiving data          |
| <b>I2C Interface(6)</b>                                    |                               |                    |      |       |         |                 |  |
| 96   | scl                           | GINT[18]           | I/O  | VDD33 | H       | Pullup/Pulldown | I2C clock  |
| 97   | sda                           | GINT[19]           | I/O  | VDD33 | H       | Pullup/Pulldown | I2C data   |
| 12   | scl <sub>2</sub>              | GINT[86]           | I/O  | VDD33 | H       | Pullup/Pulldown | I2C clock  |
| 13   | sda <sub>2</sub>              | GINT[87]           | I/O  | VDD33 | H       | Pullup/Pulldown | I2C data   |
| 32   | scl <sub>3</sub>              | -                  | I/O  | VDD33 | H       | Pullup/Pulldown | I2C clock  |
| 31   | sda <sub>3</sub>              | -                  | I/O  | VDD33 | H       | Pullup/Pulldown | I2C data   |
| <b>Serial Peripheral Interface(SPI)(24)/SCI(2)/PWMT(4)</b> |                               |                    |      |       |         |                 |  |
| 119  | ss <sub>1</sub>               | PWM[4]/GINT[10]    | I/O  | VDD33 | H       | Pullup/Pulldown | SPI chip select                                  |
| 121  | sck <sub>1</sub>              | PWM[5]/GINT[8]     | I/O  | VDD33 | H       | Pullup/Pulldown | SPI clock  |
| 120  | mosi <sub>1</sub>             | PWM[6]/GINT[9]     | I/O  | VDD33 | H       | Pullup/Pulldown | SPI master output /slave input data              |
| 118  | miso <sub>1</sub>             | PWM[7]/GINT[11]    | I/O  | VDD33 | H       | Pullup/Pulldown | SPI master input /slave output data              |
| 77   | ss <sub>2</sub>               | PWMT[0]/GINT[72]   | I/O  | VDD33 | H       | Pullup/Pulldown | SPI chip select/ pwm output                      |
| 80   | sck <sub>2</sub>              | PWMT[1]/GINT[73]   | I/O  | VDD33 | H       | Pullup/Pulldown | SPI clock /pwmt output                           |
| 78   | mosi <sub>2</sub>             | PWMT[2]/GINT[75]   | I/O  | VDD33 | H       | Pullup/Pulldown | SPI master output /slave input data /pwmt output |
| 79   | miso <sub>2</sub>             | PWMT[3]/GINT[74]   | I/O  | VDD33 | H       | Pullup/Pulldown | SPI master input /slave output data /pwmt output |
| 68   | ss <sub>3</sub>               | GINT[76]           | I/O  | VDD33 | H       | Pullup/Pulldown | SPI chip select                                  |
| 67   | sck <sub>3</sub>              | GINT[77]           | I/O  | VDD33 | H       | Pullup/Pulldown | SPI clock  |
| 66   | mosi <sub>3</sub>             | SCI3_RTS/GINT[79]  | I/O  | VDD33 | H       | Pullup/Pulldown | SPI master output /slave input data              |
| 65   | miso <sub>3</sub>             | SCI3_CTS/GINT[78]  | I/O  | VDD33 | H       | Pullup/Pulldown | SPI master input /slave output data              |
| 59   | ss <sub>spi4</sub>            | GINT[88]           | I/O  | VDD33 | H       | Pullup/Pulldown | SPI chip select                                  |
| 63   | sck <sub>spi4</sub>           | GINT[89]           | I/O  | VDD33 | L       | Pullup/Pulldown | SPI clock  |
| 62   | spi4[0]                       | GINT[90]           | I/O  | VDD33 | H       | Pullup/Pulldown | SPI data bus                                     |

## Signal Description

| Pin No.               | Name <sup>1</sup> | Alternate           | Dir. | Power             | Default | Pin Pull              | Description   |
|-----------------------|-------------------|---------------------|------|-------------------|---------|-----------------------|---|
| 60                    | spi4[1]           | GINT[91]            | I/O  | VDD33             | H       | Pullup/Pulldown       | SPI data bus  |
| 58                    | spi4[2]           | GINT[92]            | I/O  | VDD33             | H       | Pullup/Pulldown       | SPI data bus  |
| 64                    | spi4[3]           | GINT[93]            | I/O  | VDD33             | H       | Pullup/Pulldown       | SPI data bus  |
| 74                    | ss_spi5           | GINT[96]            | I/O  | VDD33             | H       | Pullup/Pulldown       | SPI chip select                                     |
| 75                    | sck_spi5          | GINT[97]            | I/O  | VDD33             | L       | Pullup/Pulldown       | SPI clock   |
| 71                    | spi5[0]           | GINT[98]            | I/O  | VDD33             | H       | Pullup/Pulldown       | SPI data bus  |
| 73                    | spi5[1]           | GINT[99]            | I/O  | VDD33             | H       | Pullup/Pulldown       | SPI data bus  |
| 72                    | spi5[2]           | GINT[100]           | I/O  | VDD33             | H       | Pullup/Pulldown       | SPI data bus  |
| 76                    | spi5[3]           | GINT[101]           | I/O  | VDD33             | H       | Pullup/Pulldown       | SPI data bus  |
| <b>SD Host/MAC(9)</b> |                   |                     |      |                   |         |                       |   |
| 86                    | sdh_dat[0]        | phy_tx[0]/GINT[131] | I/O  | VDD33             | L       | Pulldown              | SD host data/MAC transmitting data pin              |
| 84                    | sdh_dat[1]        | phy_tx[1]/GINT[132] | I/O  | VDD33             | L       | Pulldown              | SD host data/MAC transmitting data pin              |
| 89                    | sdh_dat[2]        | phy_rx[0]/GINT[133] | I/O  | VDD33             | L       | Pulldown              | SD host data/<br>MAC receiving data pin             |
| 91                    | sdh_dat[3]        | phy_rx[1]/GINT[134] | I/O  | VDD33             | L       | Pulldown              | SD host data/<br>MAC receiving data pin             |
| 85                    | sdh_cmd           | rmii_mdc/GINT[128]  | I/O  | VDD33             | L       | Pulldown              | SD host command/<br>MAC phy config clock            |
| 92                    | sdh_clk           | rmii_clk/GINT[119]  | I/O  | VDD33             | L       | Pulldown              | SD host clock/<br>MAC reference clock               |
| 83                    | sdh_det           | rmii_mdio/GINT[129] | I/O  | VDD33             | L       | Pulldown              | SD host detect/<br>MAC phy config io                |
| 88                    | sdh_wprt          | phy_txen/GINT[130]  | I/O  | VDD33             | L       | Pulldown              | SD host write protect/<br>MAC transmitting enable   |
| 90                    | sdh_cardint       | phy_rxdv/GINT[135]  | I/O  | VDD33             | L       | Pulldown              | SD host card interrupt/<br>MAC receiving data valid |
| <b>Others(6)</b>      |                   |                     |      |                   |         |                       |   |
| 109                   | WAKE UP           | -                   | I    | VCC5V             | -       | Pulldown <sup>3</sup> | wake up pin   |
| 123                   | dac_out           | -                   | O    | VDD33             | -       | -                     | dac channel output                                  |
| 127                   | adc_in[0]         | -                   | I    | VDD33             | -       | -                     | adc channel input                                   |
| 81                    | test              | -                   | O    | VDD33             | -       | -                     | chip test   |
| 101                   | PAD_XTALO         | -                   | O    | PAD_AVD<br>D_BBAT | -       | -                     | 32.768KHz oscillator<br>clock input                 |
| 100                   | PAD_XTALI         | -                   | I    | PAD_AVD<br>D_BBAT | -       | -                     | 32.768KHz oscillator<br>clock output                |

## Signal Description

| Pin No.                    | Name <sup>1</sup> | Alternate                | Dir. | Power | Default | Pin Pull        | Description                     |
|----------------------------|-------------------|--------------------------|------|-------|---------|-----------------|---------------------------------|
| <b>DCMI Interface (12)</b> |                   |                          |      |       |         |                 |                                 |
| 33                         | sensor_clkin      | GINT[115]                | I/O  | VDD33 | -       | Pullup/Pulldown | DCMI clock input                |
| 27                         | dcmi_pclk         | GINT[113]                | I/O  | VDD33 | L       | Pullup/Pulldown | DCMI clock                      |
| 22                         | dcmi_hsync        | GINT[112]                | I/O  | VDD33 | H       | Pullup/Pulldown | DCMI horizontal synchronization |
| 21                         | dcmi_vsync        | GINT[114]                | I/O  | VDD33 | H       | Pullup/Pulldown | DCMI vertical synchronization   |
| 30                         | dcmi_data[0]      | GINT[104]                | I/O  | VDD33 | H       | Pullup/Pulldown | DCMI data bus                   |
| 29                         | dcmi_data[1]      | GINT[105]                | I/O  | VDD33 | H       | Pullup/Pulldown | DCMI data bus                   |
| 25                         | dcmi_data[2]      | GINT[106]                | I/O  | VDD33 | H       | Pullup/Pulldown | DCMI data bus                   |
| 24                         | dcmi_data[3]      | GINT[107]                | I/O  | VDD33 | H       | Pullup/Pulldown | DCMI data bus                   |
| 23                         | dcmi_data[4]      | GINT[108]                | I/O  | VDD33 | H       | Pullup/Pulldown | DCMI data bus                   |
| 19                         | dcmi_data[5]      | GINT[109]                | I/O  | VDD33 | H       | Pullup/Pulldown | DCMI data bus                   |
| 18                         | dcmi_data[6]      | GINT[110]                | I/O  | VDD33 | H       | Pullup/Pulldown | DCMI data bus                   |
| 17                         | dcmi_data[7]      | GINT[111]                | I/O  | VDD33 | H       | Pullup/Pulldown | DCMI data bus                   |
| <b>LCD(20)</b>             |                   |                          |      |       |         |                 |                                 |
| 55                         | lcd_dat[0]        | mculcd_data[0]/GINT[120] | I/O  | VDD33 | L       | Pullup/Pulldown | lcd data                        |
| 57                         | lcd_dat[1]        | mculcd_data[1]/GINT[121] | I/O  | VDD33 | L       | Pullup/Pulldown | lcd data                        |
| 56                         | lcd_dat[2]        | mculcd_data[2]/GINT[122] | I/O  | VDD33 | L       | Pullup/Pulldown | lcd data                        |
| 41                         | lcd_dat[3]        | mculcd_data[3]/GINT[123] | I/O  | VDD33 | L       | Pullup/Pulldown | lcd data                        |
| 40                         | lcd_dat[4]        | mculcd_data[4]/GINT[124] | I/O  | VDD33 | L       | Pullup/Pulldown | lcd data                        |
| 38                         | lcd_dat[5]        | mculcd_data[5]/GINT[125] | I/O  | VDD33 | L       | Pullup/Pulldown | lcd data                        |
| 37                         | lcd_dat[6]        | mculcd_data[6]/GINT[126] | I/O  | VDD33 | H       | Pullup/Pulldown | lcd data                        |
| 44                         | lcd_dat[7]        | mculcd_data[7]/GINT[127] | I/O  | VDD33 | H       | Pullup/Pulldown | lcd data                        |
| 54                         | lcd_dat[8]        | mculcd_data[8]/GINT[24]  | I/O  | VDD33 | H       | Pullup/Pulldown | lcd data                        |
| 51                         | lcd_dat[9]        | mculcd_data[9]/GINT[25]  | I/O  | VDD33 | H       | Pullup/Pulldown | lcd data                        |
| 42                         | lcd_dat[10]       | mculcd_data[10]/GINT[26] | I/O  | VDD33 | L       | Pullup/Pulldown | lcd data                        |
| 43                         | lcd_dat[11]       | mculcd_data[11]/GINT[27] | I/O  | VDD33 | L       | Pullup/Pulldown | lcd data                        |
| 45                         | lcd_dat[12]       | mculcd_data[12]/GINT[28] | I/O  | VDD33 | L       | Pullup/Pulldown | lcd data                        |
| 50                         | lcd_dat[13]       | mculcd_data[13]/GINT[29] | I/O  | VDD33 | L       | Pullup/Pulldown | lcd data                        |
| 49                         | lcd_dat[14]       | mculcd_data[14]/GINT[30] | I/O  | VDD33 | L       | Pullup/Pulldown | lcd data                        |
| 48                         | lcd_dat[15]       | mculcd_data[15]/GINT[31] | I/O  | VDD33 | L       | Pullup/Pulldown | lcd data                        |
| 46                         | lcd_clcp          | mculcd_oe_n/GINT[95]     | I/O  | VDD33 | L       | Pullup/Pulldown | lcd control signal              |
| 47                         | lcd_clac          | mculcd_addr/GINT[94]     | I/O  | VDD33 | L       | Pullup/Pulldown | lcd control signal              |
| 52                         | lcd_clp           | mculcd_we_n/GINT[103]    | I/O  | VDD33 | L       | Pullup/Pulldown | lcd control signal              |

## Signal Description

| Pin No.                                       | Name <sup>1</sup>      | Alternate             | Dir. | Power | Default | Pin Pull        | Description                     |
|---|------------------------|-----------------------|------|-------|---------|-----------------|---------------------------------|
| 53  | lcd_clfp               | mculcd_cs_n/GINT[102] | I/O  | VDD33 | L       | Pullup/Pulldown | lcd control signal              |
| <b>Power Supply(11)</b>                       |                        |                       |      |       |         |                 |                                 |
| 3   | MIPIPHY_AV<br>DD       | -                     | -    | -     | -       | -               | 3.3V power input for MIPI       |
| 122   | AVDD_MCC_<br>DAC/VREFH | -                     | -    | -     | -       | -               | 3.3V power input for DAC        |
| 126   | AVDD_MCC_<br>ADC/VREFH | -                     | -    | -     | -       | -               | 3.3V power input for ADC        |
| 1/2/28/61<br>/82/87/93<br>/94/105<br>/117/125 | VDD33                  | -                     | -    | -     | -       | -               | 3.3V power output               |
| 104/113                                       | VDD_PD                 | -                     | -    | -     | -       | -               | 1.1V power output for Core      |
| 114   | VDDA                   | -                     | -    | -     | -       | -               | 1.1V power output for USB       |
| 103   | VDD18                  | -                     | -    | -     | -       | -               | 1.8V power output               |
| 14/20/26/<br>34/39                            | VDD33_FMC<br>_DATA     | -                     | -    | -     | -       | -               | 3.3V power input for SDRAM DATA |
| 107   | VCC5V                  | -                     | -    | -     | -       | -               | 3.3V power input for chip       |
| 124   | AVSS_MCC_<br>ADC/VREFL | -                     | -    | -     | -       | -               | ADC Ground                      |
| 102   | PAD_AVDD_<br>BBAT      | -                     | -    | -     | -       | -               | 3.3V power input for PCI        |
| 95  | AVDD_TSI               | -                     | -    | -     | -       | -               | 3.3V power for TSI              |
| 110/128                                       | VSS/AGND               | -                     | -    | -     | -       | -               | Ground                          |

### NOTES:

1. Shaded signals are for optional bond-out for more pin count package.
2. Pins are designed for anti-leakage.
3. Default Pull is configured by Wakeup PAD Control Register of CPM module.
4. All pullups are disconnected when the signal is programmed as an output.

## Section 4 Package information

### 4.1 General

This section provides parameters for below items:

- Package Outline Dimension (POD) of package for LQFP128

### 4.2 POD of Package LQFP128

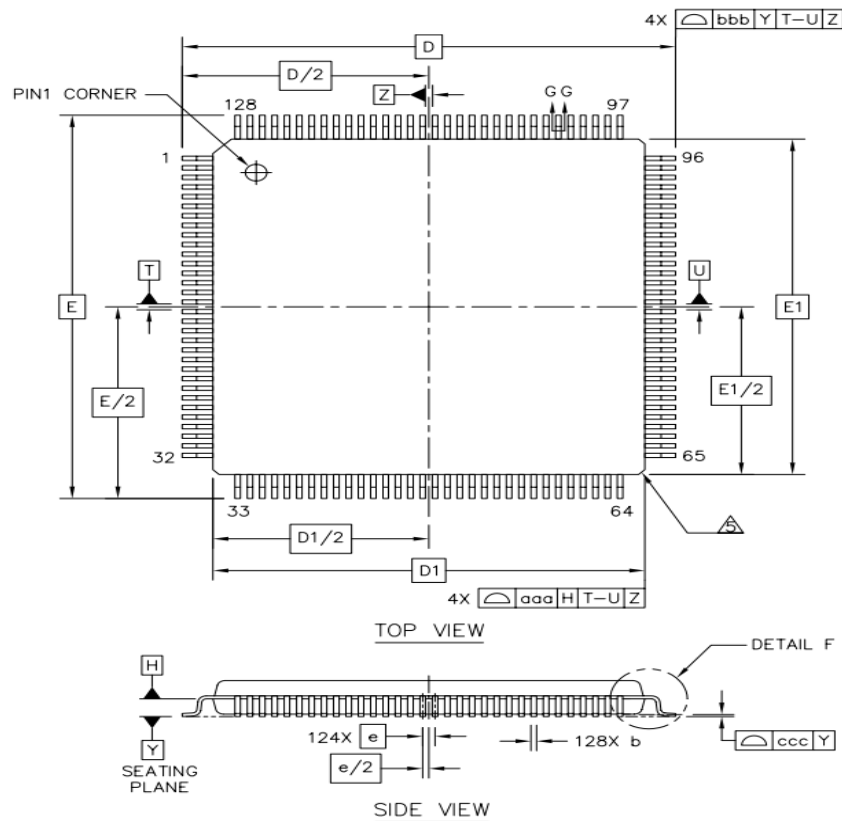


Figure 4-1 POD of Package LQFP128

**Table 4-1 POD Parameters of Package LQFP128**

|                        |   | SYMBO      | MIN     | NOM  | MAX  |
|------------------------|---|------------|---------|------|------|
| TOTAL THICKNESS        |   | A          | ---     | ---  | 1.6  |
| STAND OFF              |   | A1         | 0.05    | ---  | 0.15 |
| MOLD THICKNESS         |   | A2         | 1.35    | 1.4  | 1.45 |
| LEAD WIDTH(PLATING)    |   | b          | 0.13    | 0.16 | 0.23 |
| LEAD WIDTH             |   | b1         | 0.13    | ---  | 0.19 |
| L/F THICKNESS(PLATING) |   | c          | 0.09    | ---  | 0.2  |
| L/F THICKNESS          |   | c1         | 0.09    | ---  | 0.16 |
|                        | X | D          | 16 BSC  |      |      |
|                        | Y | E          | 16 BSC  |      |      |
| BODY SIZE              | X | D1         | 14 BSC  |      |      |
|                        | Y | E1         | 14 BSC  |      |      |
| LEAD PITCH             |   | e          | 0.4 BSC |      |      |
|                        |   | L          | 0.45    | 0.6  | 0.75 |
| FOOTPRINT              |   | L1         | 1 REF   |      |      |
|                        |   | $\theta$   | 0°      | 3.5° | 7°   |
|                        |   | $\theta 1$ | 0°      | ---  | ---  |
|                        |   | $\theta 2$ | 11°     | 12°  | 13°  |
|                        |   | $\theta 3$ | 11°     | 12°  | 13°  |
|                        |   | R1         | 0.08    | ---  | ---  |
|                        |   | R2         | 0.08    | ---  | 0.2  |
|                        |   | S          | 0.2     | ---  | ---  |
| PACKAGE EDGE TOLERANCE |   | aaa        | 0.2     |      |      |
| LEAD EDGE TOLERANCE    |   | bbb        | 0.2     |      |      |
| COPLANARITY            |   | ccc        | 0.08    |      |      |
| LEAD OFFSET            |   | ddd        | 0.07    |      |      |
| MOLD FLATNESS          |   | eee        | 0.05    |      |      |

## Section 5 Part numbering

### 5.1 BR32F4x Series Chips Naming rules

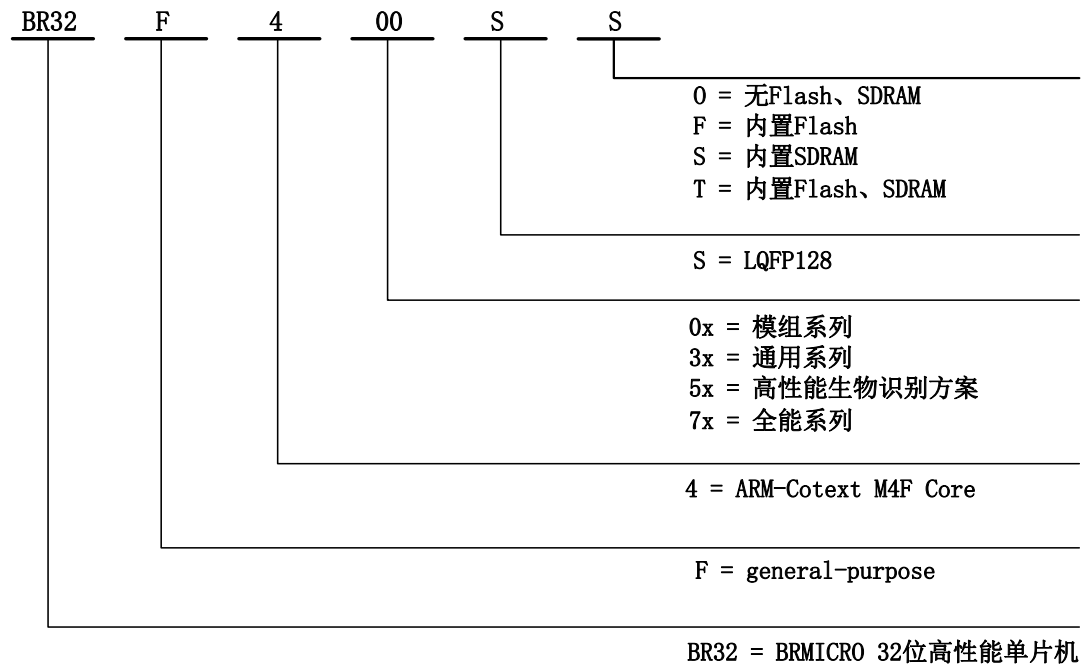


Figure 5-1 Naming rules



## Appendix A I/O DC Parameters

Table 3-1 shows the DC parameters for 3.3V I/O.

Table 3-1 DC parameters,3.3V I/O

| Parameter                            | Symbol    | Test conditions  | Minimum          | Maximum           | Units      |
|--------------------------------------|-----------|--|------------------|-------------------|------------|
| Input HIGH Level,input, and I/O pins | $V_{IH}$  | Guaranteed logic HIGH level  | 2.0              | DVDD              | V          |
| Input LOW level,input, and I/O pins  | $V_{IL}$  | Guaranteed logic LOW level   | VSS              | 0.8               | V          |
| Output HIGH voltage                  | $V_{OH}$  | VDD=minimum,DVDD= minimum, $I_{OH}^2=-2mA, -4mA,-8mA,$ and $-12mA$ | 2.4              | DVDD              | V          |
| Output LOW voltage                   | $V_{OL}$  | VDD=minimum,DVDD= minimum, $I_{OH}^2=2mA, 4mA,8mA,$ and $12mA$     | VSS              | 0.4               | V          |
| Input pull-up resistor current       | $I_{RPU}$ | $V_{PAD}=V_{IH},$<br>DVDD=minimum                                  | 50 <sup>b</sup>  | -                 | $\mu A$    |
| Input pull-up resistance             | $R_{PU}$  | $V_{PAD}=V_{IH},$<br>DVDD=minimum                                  | 9                | 19.4 <sup>e</sup> | K $\Omega$ |
| Input pull-down resistor current     | $I_{RPD}$ | $V_{PAD}=V_{IL},$<br>DVDD=minimum                                  | 50 <sup>d</sup>  | -                 | $\mu A$    |
| Input pull-down resistance           | $R_{PD}$  | $V_{PAD}=V_{IL},$<br>DVDD=minimum                                  | 6.7              | 16 <sup>e</sup>   | K $\Omega$ |
| Input hysteresis <sup>e</sup>        | $V_H$     |  | 0.2 <sup>e</sup> | -                 | V          |
| Input leakage current, non-tolerant  | $I_{PAD}$ | DVDD=maximum,<br>$V_{PAD}=0V$ or DVDD                              | -1 <sup>f</sup>  | 1 <sup>f</sup>    | $\mu A$    |
| Fail-safe Leakage Current            | $I_{PAD}$ | DVDD=0, $V_{PAD}=DVDD$<br>maximum                                  | -                | 1 <sup>g</sup>    | $\mu A$    |
| Off-State leakage current            | $I_{OZ}$  | DVDD=maximum,<br>$V_{PAD}=0V$ or DVDD                              |                  | 1.2u <sup>h</sup> | $\mu A$    |

a. Valid only when DVDD = 2.97V,process = SS,temperature = 125°C.This current is de-rated at other PVT conditions,including typical DVDD = 1.8V and 2.5V.

b. Weak pull-up current is the minimum current flowing from DVDD to PAD when

## I/O DC Parameters

- DVDD = 2.97V, process = SS, and temperature = 125°C. This value is de-rated for all the other DVDD values.
- c. The weak pull-up and pull-down resistance is the maximum resistance with the test conditions specified when DVDD = 2.97V, process = SS and temperature = 125°C.
  - d. Weak pull-down current is the minimum current flowing from PAD to ground, when DVDD = 2.97V, process = SS, and temperature = 125°C. This value is de-rated for all the other DVDD values.
  - e. Valid only when hysteresis is enabled. Simulation conditions for FF: temperature = -40°C and DVDD = 3.63V. Simulation condition for SS: temperature = 125°C and DVDD = 2.97V.
  - f. Input leakage current is the current that flows to or out of the PAD node. This leakage is measured when DVDD = 3.63V, process = FF and temperature = 125°C.
  - g. Fail-safe leakage is the current flowing from PAD to DVDD and ground when DVDD is powered down. This leakage is measured with PAD = 3.63V, Process = FF, Temperature = 125°C and DVDD = 0.
  - h. Input leakage current is the current that flows to or out of the PAD node. This leakage is measured when DVDD = 3.63V, process = FF and temperature = 125°C.

Table 3-2 shows the DC parameters for 2.5V I/O.

Table 3-2 DC parameters, 2.5V I/O

| Parameter                             | Symbol    | Test conditions                       | Minimum         | Maximum         | Units      |
|---------------------------------------|-----------|---------------------------------------|-----------------|-----------------|------------|
| Input HIGH Level, input, and I/O pins | $V_{IH}$  | Guaranteed logic HIGH level           | 1.7             | DVDD            | V          |
| Input LOW level, input, and I/O pins  | $V_{IL}$  | Guaranteed logic LOW level            | VSS             | 0.7             | V          |
| Output HIGH voltage                   | $V_{OH}$  | VDD=minimum, DVDD=minimum, $I_{OH}^2$ | 2.0             | DVDD            | V          |
| Output LOW voltage                    | $V_{OL}$  | VDD=minimum, DVDD=minimum             | VSS             | 0.4             | V          |
| Input pull-up resistor current        | $I_{RPU}$ | $V_{PAD}=V_{IH}$ , DVDD=minimum       | 25 <sup>b</sup> | -               | $\mu A$    |
| Input pull-up resistance              | $R_{PU}$  | $V_{PAD}=V_{IH}$ , DVDD=minimum       | -               | 22 <sup>e</sup> | K $\Omega$ |
| Input pull-down resistor current      | $I_{RPD}$ | $V_{PAD}=V_{IL}$ , DVDD=minimum       | 25 <sup>d</sup> | -               | $\mu A$    |
| Input pull-down resistance            | $R_{PD}$  | $V_{PAD}=V_{IL}$ , DVDD=minimum       | -               | 22 <sup>e</sup> | K $\Omega$ |
| Input hysteresis <sup>e</sup>         | $V_H$     |                                       | 0.2             | -               | V          |
| Input leakage current, non-tolerant   | $I_{PAD}$ | DVDD=maximum, VPAD=0V or DVDD         | -1 <sup>f</sup> | 1 <sup>f</sup>  | $\mu A$    |
| Input leakage current, fail-safe      | $I_{PAD}$ | DVDD=0, VPAD=DVDD maximum             | -               | 1 <sup>g</sup>  | $\mu A$    |
| Off-State leakage current             | $I_{OZ}$  | DVDD=maximum, VPAD=0V or DVDD         |                 | 1 <sup>h</sup>  | $\mu A$    |

- For derating values, see Table 3-4 on page 3-4.
- Weak pull-up current is the minimum current flowing from DVDD to PAD when DVDD = 2.25V, process = SS, and temperature = 125°C.
- The weak pull-up and pull-down resistance is the maximum resistance with the test conditions specified when DVDD = 2.25V, process = SS and temperature = 125°C.
- Weak pull-down current is the minimum current flowing from PAD to ground, when DVDD = 2.25V, process = SS and temperature = 125°C.

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- e. Valid only when hysteresis is enabled. Simulation conditions for FF: temperature =  $-40^{\circ}\text{C}$  and DVDD = 2.75V. Simulation condition for SS: temperature =  $125^{\circ}\text{C}$  and DVDD = 2.25V.
- f. Input leakage current is the current that flows to or out of the PAD node. This leakage is measured when DVDD = 2.75V, process = FF and temperature =  $125^{\circ}\text{C}$ .
- g. Fail-safe leakage is the current flowing from PAD to DVDD and ground when DVDD is powered down. This leakage is measured with PAD = 2.75V, Process = FF, Temperature =  $125^{\circ}\text{C}$  and DVDD = 0.
- h. Off-state leakage current includes Input leakage current and current from all supplies, DVDD, and VDD when DVDD = 2.75V, process = FF and temperature =  $125^{\circ}\text{C}$ .

**Table 3-3 shows the DC parameters for 1.8V I/O**

**Table 3-3 DC parameters, 1.8V I/O**

| Parameter                             | Symbol    | Test conditions                   | Minimum           | Maximum           | Units     |
|---------------------------------------|-----------|-----------------------------------|-------------------|-------------------|-----------|
| Input HIGH Level, input, and I/O pins | $V_{IH}$  | Guaranteed logic HIGH level       | $0.7 \times DVDD$ | DVDD              | V         |
| Input LOW level, input, and I/O pins  | $V_{IL}$  | Guaranteed logic LOW level        | VSS               | $0.3 \times DVDD$ | V         |
| Output HIGH voltage                   | $V_{OH}$  | VDD=minimum, DVDD=min, $I_{OH}^2$ | $0.8 \times DVDD$ | DVDD              | V         |
| Output LOW voltage                    | $V_{OL}$  | VDD=minimum, DVDD=minimum         | VSS               | $0.2 \times DVDD$ | V         |
| Input pull-up resistor current        | $I_{RPU}$ | $V_{PAD}=V_{IH}$ , DVDD=minimum   | 15 <sup>b</sup>   | -                 | $\mu A$   |
| Input pull-up resistance              | $R_{PU}$  | $V_{PAD}=V_{IH}$ , DVDD=minimum   | 11.2              | 32.4 <sup>e</sup> | $K\Omega$ |
| Input pull-down resistor current      | $I_{RPD}$ | $V_{PAD}=V_{IL}$ , DVDD=minimum   | 15 <sup>d</sup>   | -                 | $\mu A$   |
| Input pull-down resistance            | $R_{PD}$  | $V_{PAD}=V_{IL}$ , DVDD=minimum   | 9.4               | 32.4 <sup>e</sup> | $K\Omega$ |
| Input hysteresis <sup>e</sup>         | $V_H$     |                                   | $0.1 \times DVDD$ | -                 | V         |
| Input leakage current, non-tolerant   | $I_{PAD}$ | DVDD=maximum, VPAD=0V or DVDD     | -1 <sup>f</sup>   | 1 <sup>f</sup>    | $\mu A$   |
| Input leakage current, fail-safe      | $I_{PAD}$ | DVDD=0, VPAD=DVDD maximum         | -                 | 1 <sup>g</sup>    | $\mu A$   |
| Off-State leakage current             | $I_{OZ}$  | DVDD=maximum, VPAD=0V or DVDD     |                   | 1 <sup>h</sup>    | $\mu A$   |

- a. For derating values, see Table 3-4.
- b. Weak pull-up current is the minimum current flowing from DVDD to PAD when DVDD = 1.62V, process = SS, and temperature = 125°C.
- c. The weak pull-up and pull-down resistance is the maximum resistance with the test conditions specified when DVDD = 1.62V, process = SS and temperature = 125°C.
- d. Weak pull-down current is the minimum current flowing from PAD to ground,

## I/O DC Parameters

- when DVDD = 1.62V, process = SS and temperature = 125°C.
- Valid only when hysteresis is enabled. Simulation conditions for FF: temperature = -40°C and DVDD = 1.98V. Simulation condition for SS: temperature = 125°C and DVDD = 1.62V.
  - Input leakage current is the current that flows to or out of the PAD node. This leakage is measured when DVDD = 1.98V, process = FF and temperature = 125°C.
  - Fail-safe leakage is the current flowing from PAD to DVDD and ground when DVDD is powered down. This leakage is measured with PAD = 1.98V, Process = FF, Temperature = 125°C and DVDD = 0.
  - Off-state leakage current includes Input leakage current and current from all supplies, DVDD, and VDD when DVDD = 1.98V, process = FF and temperature = 125°C.

### Table 3-4 shows simulated drive current at slow PVT conditions

Table 3-4 DC driver current for PBIDIR\_33\_33\_FS\_DR<sup>a</sup>

| Drive strength | I <sub>OH</sub> ,DVDD =3.3V | I <sub>OL</sub> ,DVDD =3.3V | I <sub>OH</sub> ,DVDD =2.5V | I <sub>OL</sub> ,DVDD =2.5V | I <sub>OH</sub> ,DVDD =1.8V | I <sub>OL</sub> ,DVDD =1.8V | Unit |
|----------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|------|
| 2              | 2.45                        | 2.43                        | 1.87                        | 1.87                        | 1.35                        | 1.28                        | mA   |
| 4              | 4.88                        | 4.96                        | 3.73                        | 3.83                        | 2.7                         | 2.64                        | mA   |
| 8              | 9.76                        | 9.84                        | 7.47                        | 7.59                        | 5.4                         | 5.22                        | mA   |
| 12             | 14.6                        | 14.7                        | 11.18                       | 11.36                       | 8.1                         | 7.84                        | mA   |

- PVT corners that are used for simulation:  
 3.3V SS/2.97V/125°C.  
 2.5V SS/2.25V/125°C.  
 1.8V SS/1.62V/125°C.  
 In 3.3V, I<sub>OH</sub>, and I<sub>OL</sub> measured with V<sub>DS</sub>=0.4V.

# Appendix B Preliminary Electrical Characteristic

## 0.1 General

This section provides electrical parametrics and electrical ratings for the microcontroller unit.

## 0.2 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which the Chip can be exposed without permanently damaging it. See **Table 0-1**.

The Chip contains circuitry to protect the inputs against damage from high static voltages; however, do not apply voltages higher than those shown in the table. Connect unused inputs to the appropriate voltage level,  $V_{DDH}$ . This device is not guaranteed to operate properly at the maximum ratings. Refer to **0.4, 0.4, Table 0-3, Table 0-4** for guaranteed operating conditions.

**Table 0-1 Absolute Maximum Ratings**

| Num | Rating                      | Symbol    | Value       | Unit |
|-----|-----------------------------|-----------|-------------|------|
| 1   | Operating temperature range | $T_{OPT}$ | -25 to +65  | °C   |
| 2   | Storage temperature range   | $T_{STG}$ | -40 to +125 | °C   |

### 0.3 Electrostatic Discharge (ESD) Protection

**Table 0-2 ESD Protection Characteristics**

| <b>Parameter<sup>1,2,3,4,5</sup></b> | <b>Symbol</b> | <b>Value</b> | <b>Units</b> |
|--------------------------------------|---------------|--------------|--------------|
| ESD target for human body model      | HBM           | 2000         | V            |
| Latch Up                             | Latch UP      | 200          | mA           |

NOTES:

1. This report will be invalid if reproduced in whole or in part.
2. This report refers only to the specimen(s) submitted to test, and is invalid if used separately.
3. This report is ONLY valid with the examination seal and signature of this institute.
4. The tested specimen(s) will only be preserved for thirty days from the date issued, if not collected by the applicant.
5. The failure criteria of all ESD tests should be based on the result of parametric and functional testing conducted by the customer, which follows the statement of international standards. Thus, the judgment of the curve traces provided in this report is for reference ONLY.



## 0.4 DC Electrical Specifications

Table 0-3 DC Electrical Specifications(3.3V)

| Parameter   | Symbol    | Min  | Typical | Max  | Unit    |
|---|-----------|------|---------|------|---------|
| Supply Voltage                                    | $V_{DDH}$ | 3    | 3.3     | 3.6  | V       |
| Input High Voltage                                | $V_{IH}$  | 2    | —       | DVDD | V       |
| Input Low Voltage                                 | $V_{IL}$  | VSS  | —       | 0.8  | V       |
| Output High Voltage                               | $V_{OH}$  | 2.4  | —       | DVDD | V       |
| Output Low Voltage                                | $V_{OL}$  | VSS  | —       | 0.4  | V       |
| Pull-up Resistor current                          | $R_{PU}$  | 50   | —       | —    | $\mu A$ |
| Input Leakage Current@DVDD=max,VPAD=0 o DVDD      | $I_{IN}$  | -1.2 | —       | 1.2  | $\mu A$ |
| Fail leakagecurrent @DVDD=0,VPAD=DVDD=max         | $I_{PAD}$ | —    | —       | 1.2  | $\mu A$ |
| Off_state leakage current@DVDD=max,VPAD=0 or DVDD | $I_{OZ}$  | —    | —       | 1.2  | $\mu A$ |

## 0.5 Power Consumption

**Table 0-4 power consumption<sup>1</sup>**

| Parameter                            | power consumption |
|--------------------------------------|-------------------|
|                                      | 400MHz            |
| CPU run                              | 97mA              |
| CPU and peripherals run <sup>1</sup> | 129mA             |
| CPU and SDRAM run <sup>2</sup>       | 96mA              |
| CPU,SDRAM and peripherals run        | -                 |
| LOWPOWER MODE <sup>3</sup>           | 14mA              |
| POWEROFF1.0 MODE <sup>4</sup>        | -                 |
| POWEROFF2.0 MODE <sup>5</sup>        | 185uA             |

NOTES:

1. All the peripherals are operated in fastest speed.

2. CPU:SDRAM=4:1 in speed.

3. Chip poweron and clock stop.

wakeup source: USI,I2C,EPORT,USB RESUME,TSI TOUCH,TIME COUNTER, RTC,WK PAD,USBDET,POR,PCI

4. Only TSI run in poweroff 1.0 mode.

wakeup source: EPORT0,TSI TOUCH,RTC,WK PAD,USBDET,POR,PCI

5. Only PCI poweron.

wakeup source: WK PAD,USBDET,POR

NOTES:

1. All the data are typical results.

## 0.6 AC Timing

### 0.6.1 SPI Interface

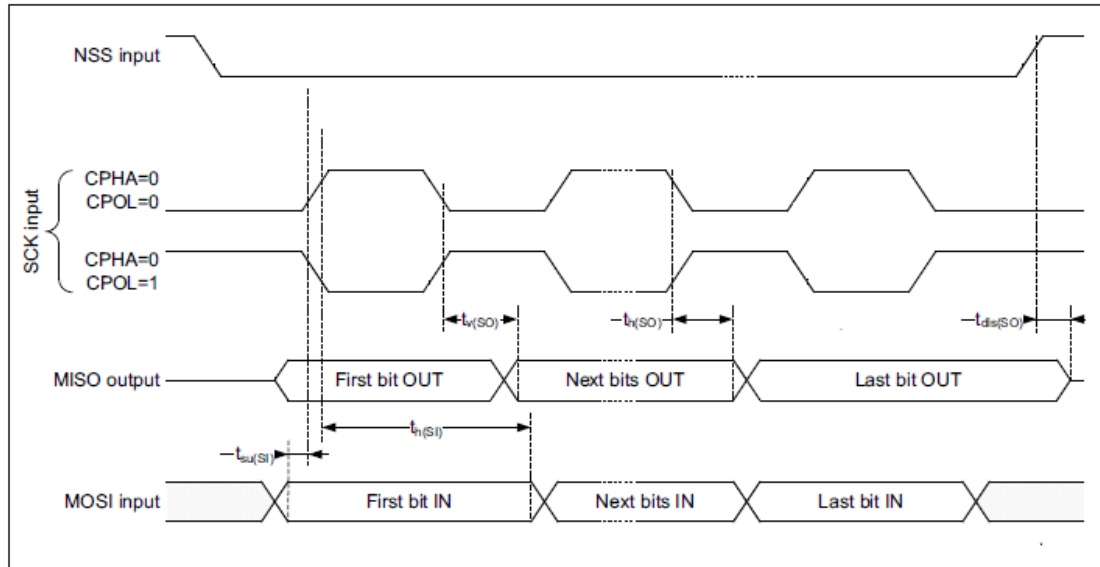


Figure 0-1 SPI timing diagram

Table 0-5 SPI characteristics

| Symbol        | Parameter                | condition         | min | typ | max   | Unit |
|---------------|--------------------------|-------------------|-----|-----|-------|------|
| $f_{sck}$     | SPI clock frequency      | VCC3.3V,VDD 1.1V  | -   | -   | 50    | MHz  |
|               |                          | VCC3.3V,VDD 1.23V | -   | -   | 62.5  |      |
| $t_{su(SI)}$  | Data input setup time    | VCC3.3V,VDD1.1V   | -   | 3.9 | 6.9   | ns   |
| $t_{h(SI)}$   | Data input hold time     | VCC3.3V,VDD1.1V   | -1  | 0   | -     |      |
| $t_{dis(SO)}$ | Data output disable time | VCC3.3V,VDD1.1V   | 5.9 | 8   | 11.9  |      |
| $t_{v(SO)}$   | Data output valid time   | VCC3.3V,VDD1.1V   | -   | 9.8 | 14.95 |      |
| $t_{h(SO)}$   | Data output hold time    | VCC3.3V,VDD1.1V   | 2.3 | 3.9 | -     |      |

## 0.6.2 SSI(QSPI) Interface

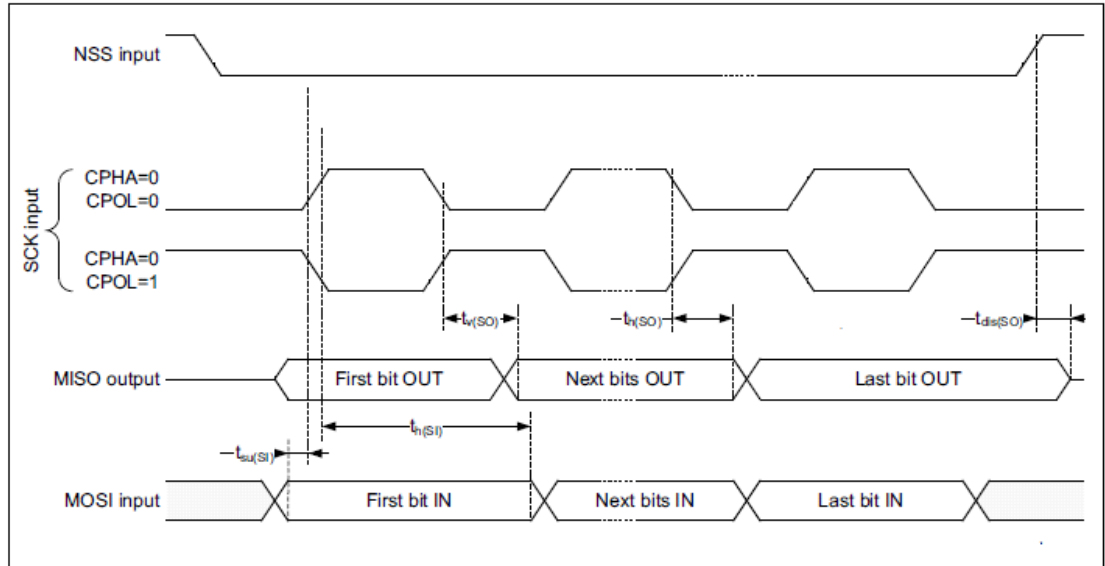


Figure 0-2 SSI(QSPI) timing diagram

Table 0-6 SSI(QSPI) characteristics

| Symbol        | Parameter                | condition         | min | typ | max | Unit |
|---------------|--------------------------|-------------------|-----|-----|-----|------|
| $f_{sck}$     | SSI clock frequency      | VCC3.3V,VDD 1.1V  | -   | -   | 100 | MHz  |
|               |                          | VCC3.3V,VDD 1.23V | -   | -   | 125 |      |
| $t_{su(SI)}$  | Data input setup time    | VCC3.3V,VDD1.1V   | 2   | -   | -   | ns   |
| $t_{h(SI)}$   | Data input hold time     | VCC3.3V,VDD1.1V   | 3   | -   | -   |      |
| $t_{dis(SO)}$ | Data output disable time | VCC3.3V,VDD1.1V   | -   | -   | 7   |      |
| $t_{v(SO)}$   | Data output valid time   | VCC3.3V,VDD1.1V   | -   | -   | 6   |      |
| $t_{h(SO)}$   | Data output hold time    | VCC3.3V,VDD1.1V   | 0   | -   | -   |      |